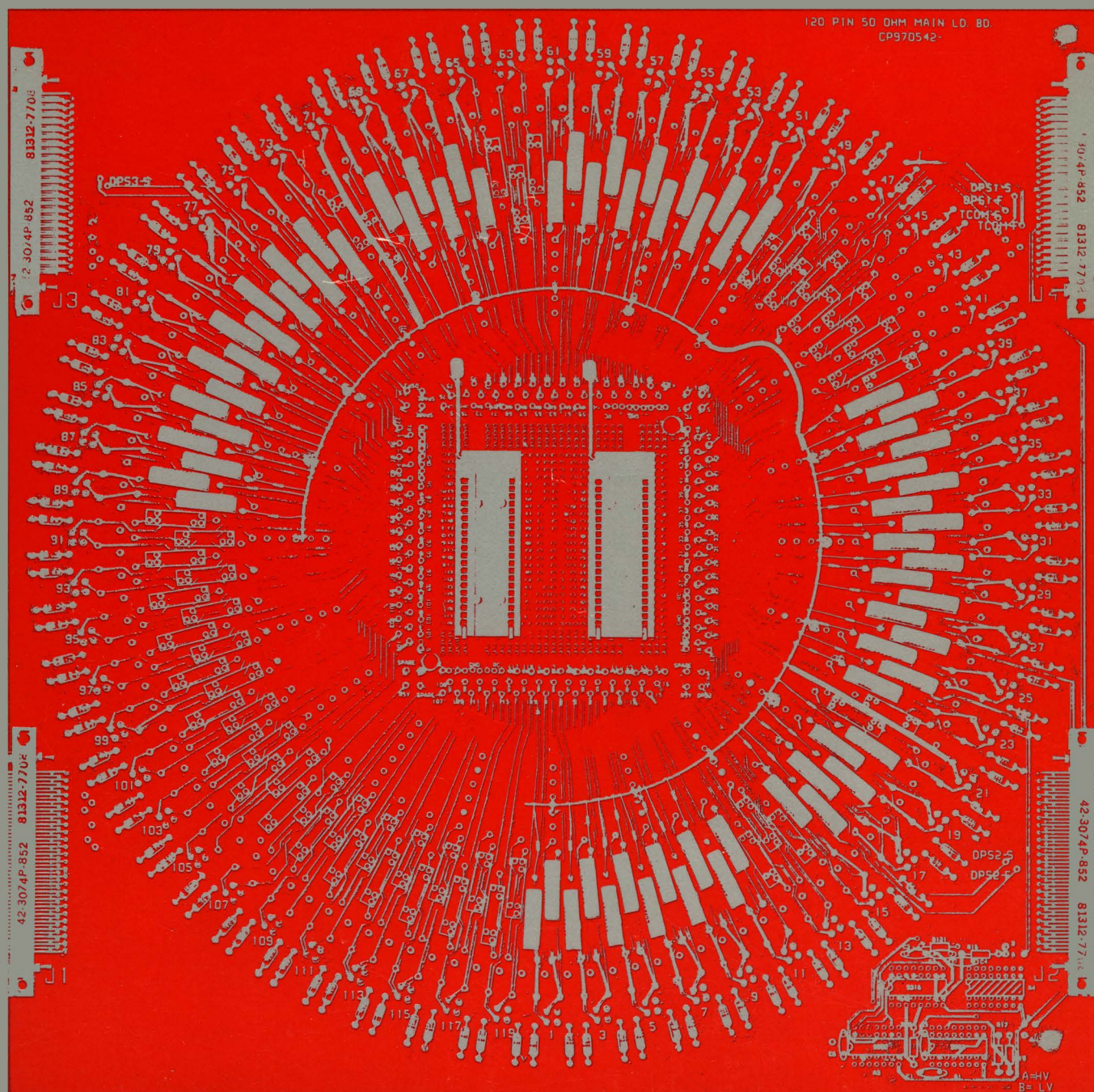


FAIRCHILD

SENTRY VIII

General Purpose LSI/VLSI Test System



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**General Purpose
LSI/VLSI
Test System**



Test Systems Group

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SENTRY VIII

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Introduction

This document is designed to provide general technical information for the Fairchild Sentry VIII Semiconductor test system. This document is divided into two parts. The first part contains the general information describing the system and its enhancements. The second part contains detailed specifications designed to help the engineer evaluate the performance criteria of the test system.

The Fairchild Test Systems Group Sentry VIII is primarily designed for engineering characterization, start-up VLSI production and incoming inspection and Q.A. Its success in solving GSI, MSI, and VLSI test problems has been unparalleled by any other commercial tester on the market. More manufacturers and users in the world use Sentry to solve their test problems than any other tester of its type.

The Sentry VIII combines the power of the Sentry VII test system with 120 pin testing capability to create the most advanced VLSI test system in the industry. The Sentry VIII can be configured to test any of today's state-of-the-art circuits and has the future designed in to meet tomorrow's VLSI testing challenges, whether they be RAMS, microprocessors, ECL bit slices or random logic circuits.

Five years of field proven success has demonstrated the flexibility and power of the Sentry VIII. Fairchild has delivered Sentry VIII systems to customers throughout the world and has converted user's suggestions into system enhancements that are culminated in today's Sentry VIII. As these features are incorporated into the Sentry VIII, the user's test program will never become obsolete because Sentry software is designed to make the test programs upward compatible.

The 60 pin to 120 pin performance board adaptor is a further example of Fairchild's commitment to nonobsolescence of its products. The performance board adaptor allows the user to immediately transfer existing Sentry test programs to the Sentry VIII with no hardware or software changes.

1.1 Sentry VIII General Description

The Sentry VIII is a universal test system, designed to operate in a multitude of environments to meet a multitude of testing needs. For the engineer, the Sentry VIII combines over 50 man-years of sophisticated software development and high-speed hardware technology with an extensive customer-feedback loop, resulting in a powerful yet flexible characterization and analysis tool. For the quality control engineer, Shmoo plots, histograms, delta measurements, extensive datalogging and data manipulation are part of the standard Sentry software. Environmental chambers and handlers are readily interfaced to the high speed test head to aid in component evaluation.

The Sentry hardware is modularly designed to enable each customer to select that configuration which best suits present needs.

The system permits expansion in various test areas through the addition or selection of different test stations. The basic building block (the FST-2 computer with 64K 24-bit word memory), the Video Keyboard Terminal, and other peripherals, have been designed to control and operate up to two 120 pins test stations.

The extensive number of software routines available to the user gives the Sentry an unparalleled ability within the device characterization and data analysis field. This ability includes plots of mathematical functions, parametric distributions, three-dimensional distributions (commonly referred to as composite Shmoo and matrices with various X and Y parameters).

The Sentry VIII test station electronics combined with the high speed test controller provide the capability to do functional testing at a 10MHz rate and DC parametric testing at rates up to 1000 tests/second. These tests are performed at the programmed rate by inputting data to the device-under-test (DUT) and comparing outputs with expected output values are stored in a local memory in the high speed controller.

The Sentry system will support high voltage and/or high speed test stations. The high voltage test stations of the Sentry include true universal capability for all 120 active test pins. Each test pin under software control may be assigned as an input driver, output comparator, input clock, bias supply, load or input/output pins. For characterization and testing of TTL, ECL, NMOS and other high speed, low level logic families, the high speed test station is available. This test station features faster rise and fall times and adjustable comparator skew times making it ideal for testing the high speed device technologies. The precision measurement unit may be connected to any device pin to measure or datalog the voltage/current parametric characteristics of the device under test.

The local memory is a specialized processor which consists of bipolar random access memory, control registers, and instruction set. One local memory channel is assigned to each of the 120 DUT pins. By using RAMs for local memory, the FST-2 computer can update the functional patterns in local memory while testing is going on at the programmed rate with no break in in the test vectors applied to the DUT.

Under standard system software control, local memory can be segmented into major and minor loops with separate start and stop addresses and loop counts. With the Sequence Processor, the Sentry further condenses long test patterns for optimum use of local memory by modifying register definitions on-the-fly, nesting subroutines upto to 16 deep, and doing clock-bursts. The Sentry VIII Pattern Processor for testing large scale memory chips also makes maximum use of local memory, by offering independent X and Y addressing, split-cycle timing, topological scrambling, hardwired data equations, and pseudo-random data generation.

Several registers within the high speed controller allow control of each DUT pin while testing at the programmed rate. Two pairs of mask and I/O definition registers allow changing of the DUT pin I/O definition and "care"/"don't care" conditions on-the-fly. Another register controls the selection of the input reference voltage pair to the DUT inputs. Up to four pairs of input reference voltages are available for selection. Other registers control data driver mode definitions, record failures and invert data patterns.

Output data of the DUT is checked via the high speed comparator for level and polarity and with the stored expected output pattern and sequence of the local memory associated with that pin.

The test instruction set for control of the bias and reference supplies, the system control registers, the timing generators, local memory and pin electronics, as well as the functional pattern, are stored as part of the device test program. The local memory instruction set, the timing generator conditions and the precision measurement unit conditions as well as the bias supply conditions are under complete control of the user's device program.

The Sentry VIII focuses on the testing and data analysis requirements for state-of-the-art VLSI devices. The Sentry VIII includes three hardware groups which will be discussed in greater detail in this document, they are:

- Peripherals
- Central control console
- High speed test station group

System Peripherals and External Interfaces

The Sentry system software supports any combination of available peripherals and external interfaces. The peripheral equipment available with the system includes:

- Video Keyboard Terminal
- Magnetic Tape Unit
- Medium-Speed Line Printer
- High-Speed Line Printer
- Card Reader
- Disc Memory Unit

The external interfaces that are available include:

- Data Set Interface
- Instrumentation Bus Interface

All peripherals can be referenced by name in the software, which provides for the addition of more peripherals without basically changing the operation of the system.

2.1 System Peripherals

2.1.1 Video Keyboard Terminal (VKT)

The VKT is the primary operator/system interface device. It consists of a separate keyboard and a CRT display unit. The keyboard unit allows the user to:

- Initialize and interface with the system and user software
- Select operating parameter
- Enter system command
- Build and edit program and user file
- Compile and execute user program
- Visually display user inputs/outputs and system error messages

Program statements and system control statements entered on the keyboard are transmitted to the computer and simultaneously displayed on the VKT display. The VKT provides a visual record of all keyboard operations and on call, displays all test programs, test station registers,

and test results for functional and parametric testing. The general characteristics of the VKT include:

Character Set	63 USACII alphanumeric characters, space, and special symbol.
Data Transmission Rate	9600 baud
Keyboard	Solid state with teletype key arrangement.

2.1.2 Dual VKT Option

To take full advantage of the foreground/background feature of the MASTR software, a dual VKT option is available. This option allows the user to perform interactive background operations while the Sentry is testing devices in the foreground. This second VKT allows the user to fully utilize the power of the Sentry test system, thereby reducing overhead costs.

2.1.3 Magnetic Tape Unit

The standard magnetic tape unit provides a fast means of loading the system software and of storing and retrieving user programs. An additional magnetic tape unit may be added to the system as an option. The general characteristics of the magnetic tape unit include:

Tape Speed	Normal READ/WRITE 24 ips Rewind and Fast Forward 150 ips
Tape Size (maximum)	1/2 inch by 1.5 mil by 2400 feet mounted on a 10-0/2 inch reel (IBM or NAB)
Recording Density (9-track)	800 bpi
Format	IBM-Compatible ANSCII format
Recording Mode	NRZI

2.1.4 Medium Speed Line Printer

The medium-speed line printer is available for applications requiring printed test data. This allows the user to obtain high-quality hard-copy printouts of test programs, error messages and the contents of any desired unprotected file. The general characteristics of the medium-speed line printer include:

Print Rate	300 lpm for standard-size characters 170 lpm for double-height characters 240 lpm when underlining or printing lower-case characters with descenders (tails below the line)
Character Format	132 characters per line 10 characters per inch horizontal 6 or 8 characters per inch vertical
Character Set	Standard 64 character ASCII set
Character Registration	0.005 inches horizontal or vertical
Character Structure	9 x 7 dot matrix
Paper Type	Pin feed continuous fanfold. Single-part 15-pound to 100-pound. Up to six-part NCR or carbon forms of average quality, eight-part forms of premium quality.
Paper Width	4-1/2 to 16 inches
Advance Speed	6 lpi at 33 ms. 8 lpi at 25 ms.

2.1.5 High Speed Line Printer

For those applications requiring large amounts of printed data, the high speed line printer is recommended. This free standing printer is capable of printing 600 lines per minute using the drum printing technique. The general characteristics of the high speed line printer include:

Print Rate	600 lpm (minimum)
Character Format	136 characters per line
Character Set	Standard 64 character ASCII set
Character Registration	0.1 inch horizontal between centers 0.167 inch vertical line spacing
Paper Type	Pin feed continuous fanfold with 11 inches between folds
Paper Width	4 to 16.75 inches
Advance Speed	25 ms (maximum)

2.1.6 Card Reader

The card reader provides a fast, convenient and flexible means of loading test programs. The unit reads 80-column punched data processing cards, column-by-column. The card reader operates in a remote mode in response to commands from the computer. Data is transferred from the cards by the card reader and transmitted as electrical pulses to the FST-2 computer. The general characteristics of the card reader include:

Card Storage	600 cards, maximum
Card Reading Rate	318 cards/minute
Time Between Cards	60 ms
Time Between Columns	2 ms

2.1.7 Disc Memory

The disc memory operates with a fast, fixed head to provide instant access to any test program in the user's device library, to remove memory size restrictions, and to store the operating software, diagnostics and self-check programs. The disc memory unit is an extension of the main memory. It has one rotating disc and uses the one-head-per-track principle. The unit is self-contained, requiring only an external AC power source and an external input/output control. The characteristics of the disc memory unit include:

Storage Capacity	768,000 24-bit words
Transfer Rate	113,000 words/second
Average Access Time	17 ms
Disc Rotation Speed	1745 rpm

2.2 External Interfaces

2.2.1 Data Set Interface

The data set interface is available to provide a communications link to data processing facilities. This link may be used for down-loading test programs from a host CPU or up-loading test result data to the host for storage, in-depth statistical analysis and user defined graphic reports.

The data set interface is fully compatible with the EIA standard RS232C and Bell System 202S operating disciplines. Data is transmitted asynchronously in ASCII or packed Binary at switch-selectable data rates of 110 to 9600 baud. A communications link may be established in a local null-modem configuration when the host CPU is adjacent to the Sentry test system. If the host CPU is remote, the data set interface may be used with a Bell system 202S Data Set to establish a 1200-baud communications link over dial-up facilities. Data integrity is assured by cross-parity error checking on all messages. If an error is detected in any message, the message is automatically retransmitted and verified.

2.2.2 Instrumentation Bus Interface

The instrumentation bus interface is an industry standard external interface, which, like the data set interface, provides greater system flexibility. The instrumentation bus interface communicates with external instrumentation compatible with ANSI/IEEE Standard 488-1975.

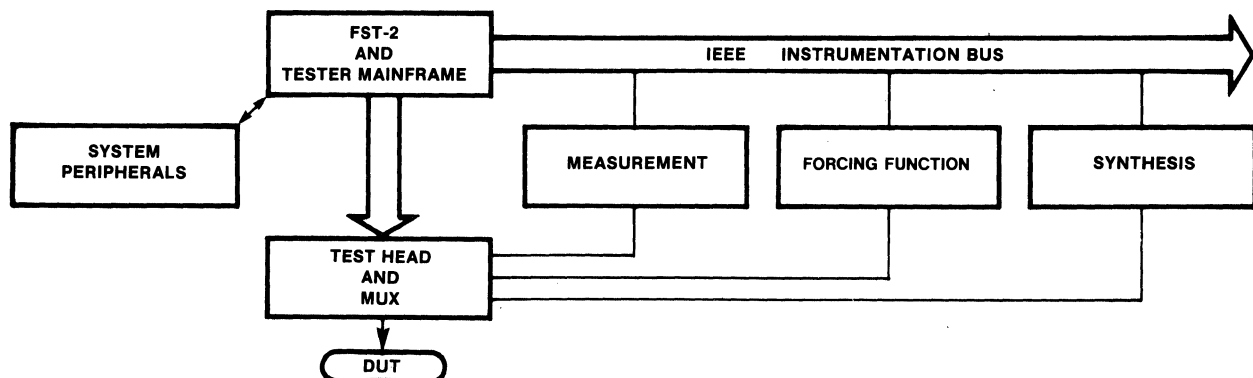
The bus functions of talker, listener, and controller may be invoked by the operator from the VKT or by a FACTOR program. Up to 14 external instruments may be connected to the bus and programmed directly through the instrumentation bus interface.

The instrumentation bus interface is highly recommended for Sentry applications that require auxiliary instrumentation beyond the basic capabilities of the tester. Wavetek, Dana, Fluke, Systron Donner, Tektronix, Hewlett-Packard, Phillips and Fairchild presently manufacture instrumentation that complies with the IEEE standard. Some of the instrument functions available include:

- Frequency synthesizers
- Signal generators
- Counters
- Multimeters
- Crosspoint matrix controllers
- Word generators
- Function generators
- Capacitance bridges
- Pulse generators
- UHF/VHF test sets
- Programmable filters
- Programmable calibrators

Figure 2-1 illustrates a typical application.

Fig. 2-1 Instrumentation Bus Interface Application



Central Control Console

The Central Control Console Mainframe houses the FST-2 Computer, Reference Voltage Supplies, Device Power Supplies, Precision Measurement Unit, and High Speed Controller, all in one cabinet.

3.1 FST-2 Computer

The nucleus of the Sentry family is Fairchild's FST-2 general purpose 24-bit word computer which controls the complete system. Using FACTOR, an English-like test program language, the computer transmits control data, and receives subsystem status reports, interrupt requests and test data. The features of the FST-2 are:

- 24-bit data word
- 1.75 microsecond memory-cycle time
- 64K of semiconductor storage, expandable in 16K modules up to 196K
- Dual memory-access via two memory buse
- Random direct memory access, stored by/retrieved at 571,000 words per second per memory bus
- Separate interface control between memory modules and CPU or tester
- Interrupt sub-system for communications and data transfer between CPU and peripheral units via accumulator bus
- 16 external interrupt channels and a maximum of 64 memory interrupt locations
- 7 index registers for address modification and a relocation register
- Indirect addressing for most instructions
- A six-bit operation code for the following types of instructions
 - load and store
 - arithmetic
 - logical operations
 - register and status
 - conditional and unconditional branch
 - transfer-of-control
 - shift
 - input/output

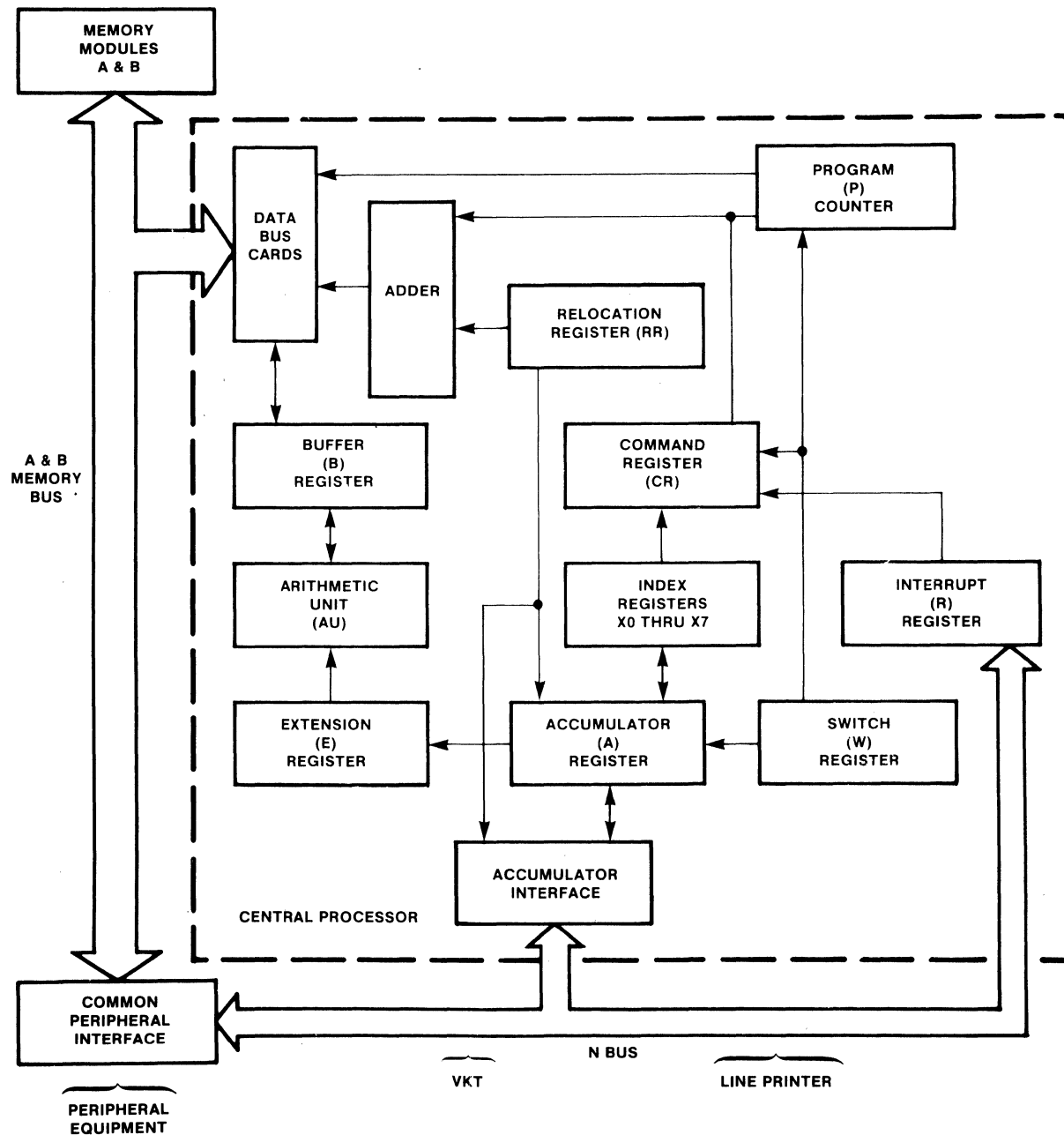
- The FST-2 Computer is a general purpose digital computer consisting of three subsystems:

central processing unit (CPU)
memory
interface

Controls are available on the test station panel for controlling the FST-2 during normal operation. This panel provides all controls and indicators for the FST-2. The switch register provides a means of manually setting up a 24-bit word and reading the contents of various working registers.

The FST-2 uses semiconductor memory. A minimum memory subsystem is 64K 25-bit words (bit 25 is memory parity) and can be expanded in in-

Fig. 3-1 FST-2 Simplified Block Diagram



crements of 16K words up to 196,608 words. Operating in a Direct Memory Access mode, the computer minimizes test execution time by direct loading of local memory. By increasing CPU memory capacity test throughput improvement factors can be obtained. The A and B memory data buses are interfaced to the memory and primarily used for transmitting functional test data at memory speeds to the tester. Both of these memory buses may be in operation at the same time.

The basic configuration for the FST-2 is shown in figure 3-1.

3.2 Reference Voltage Supplies (RVS)

The Reference Voltage Supplies (RVS's) provide the "1" and "0" logic levels to the drivers and detectors. The system is available with up to six pairs of RVS supplies contained on 6 boards (one pair per board). The driver RVS's are designated E0/E1, EA0/EA1, EB0/EB1 and EC0/EC1. The comparator and reference supplies are designated S1/S2 and SA0/SA1. Systems equipped with the high speed test stations are supplied with E0/E1, EA0/EA1, EB0/EB1, S0/S1 and SA0/SA1 reference supplies. Refer to specification section for detailed range information.

3.3 Device Power Supplies (DPS)

The mainframe also contains up to three Device Power Supplies (DPS). These supplies provide programmable voltages and programmable currents to the test station for parametric testing.

Device Power Supplies provide the power to activate the Device-Under-Test (DUT) when connected externally at the performance board. The supplies can be programmed to force a voltage with a programmable current trip. On the high voltage test station the device power supply can be programmed to any pin(s) on the DUT performance board through a buffer driver on the pin electronics card with a drive capability of 100 mA, per pin. The device power supply can also be connected directly to the performance board to provide drive capabilities of 1 A. The specification section provides complete specifications of the DPS when buffered and channeled through the pin electronics. The high speed test station device power supplies and tester common are available only at the performance board.

The device power supplies are programmable in two ranges and polarity with an optional third range. Magnitude is contained in 10 bits; range is contained in 2 bits and the sign is contained in 1 bit. The specifications of the device power supplies apply when the device power supplies are brought to the test head through the performance board rather than through the pin electronics. The specifications section provides detailed range information.

3.4 Current Trip Detector (DPT)

The digitally programmed current trip detector (DPT) is programmable in two ranges and acknowledges current flow direction according to the polarity of the device power supplies. The value of the trip level is stored in a 12-bit binary register. Refer to specification section for detailed range information.

3.5 Precision Measurement Unit (PMU)

The Precision Measurement Unit (PMU) is an instrument which, under program control, can be connected to an individual pin of the DUT to make a quantitative voltage or current measurement at that point. This unit is used for DC parametric or DC GO/NO-GO testing. The PMU can also apply (force) a precise, program-specified voltage or current to any desired pin of the DUT. In practice, these two operations are performed simultaneously; a voltage is applied and a measurement is made of the

resulting current flow, or, a current is forced and the voltage is measured. The use of the PMU voltage clamp offers the user protection from over voltage due to programming errors or voltage compliance problems. Refer to specification section for voltage clamping information.

The PMU is a precision, digitally programmed forcing and sensing unit with 10 bits for magnitude, 2 bits for range, 1 bit for polarity, and 1 bit for voltage or current. Maximum capacitive loading is 0.01 F. Recommended calibration check period is one month.

The PMU can also be used to make a variety of measurements within the test system itself, such as measuring test head analog reference voltages and functional test voltages, as well as voltages at certain of the test points located on the printed circuit cards. This is done automatically during system self-check under the control of diagnostic programs. Thus, the PMU is also a trouble-shooting and maintenance aid.

The operation of the PMU is controlled mainly by the contents of four registers.

- PPS (Precision Power Supply) register
- DCT (DC Trip) register
- PSL (Precision Sense Level) register
- PA (Pin Address) register

The PPS register holds the information determining the value of the voltage (or current) to be forced. This includes polarity, range, magnitude, and whether the forced quantity is voltage or current.

The DCT register is used to hold the information fed into a DAC which is part of the circuitry for the analog-to-digital conversion of the measured current (or voltage). When this conversion is made, the measured quantity is contained in this register in digital form. Polarity, range, and magnitude information are also present.

The PSL register is used to hold the information establishing the operating range for voltage or current measurements by the PMU, and specifying whether it is current or voltage that is to be measured. The PSL register also holds the information specifying voltage clamp values. These values are upper and/or lower limits on the allowable voltage at the PMU output; at the pin of the DUT. This provides protection for the DUT. For example, a programming error may cause the PPS register to specify a harmfully high voltage to be applied to the pin of the DUT. In this case the voltage clamp circuit, programmed with limit values held in the PSL register, provides the required compensation within the voltage feedback loop, so the PMU output voltage does not violate these limits.

The PA register holds the information controlling the connection of the PMU to the appropriate pin of the DUT or to the appropriate internal node within the test system. The bits of the PA register are the pin address. Refer to the specifications section for detailed PMU voltage and current range information.

3.6 2V/2mV RVS-DPS-PMU Option

The optional 2V/2mV capability of the Sentry provides increased voltage resolution for the low voltage technologies (TTL, ECL, and I²L). The optional 2V/2mV range is incorporated into the RVS and DPS, and the 1V/1mV range of the PMU is changed to 2V/2mV. Refer to the specification for detailed PMU 2V/2mV information.

3.7 High Speed Controller

The circuitry that controls the digital data originating from the CPU memory is contained within the high speed controller. The controller provides up to 16 timing generators (four for strobe and twelve for clock and data timing).

The basic system allows complete functional testing at 10 MHz data rate at either the wafer probe or final test level, depending upon the station selected. The system also performs DC parametric testing (stress, leakage, continuity) at a rate of up to 300 tests per second in addition to AC measurement.

The station controller gives the PMU the ability to perform stress, leakage, parameter, and loading measurements and subsequent datalogging. It also provides up to 60 x 4096-bit local memory pattern depth at each pin electronics for functional testing; expandable to a maximum of 120 x 4096 bits.

The high-speed controller has enable latches which allow the system to continue testing after a "fail" and provide the accumulated pin failures at the end of a test cycle. An external sync capability is also provided to allow testing of "self-timing" devices.

One high speed controller is allowed per system. The controller may have up to two high-voltage test stations or two high-speed test stations or two test stations of any type.

The high-speed registers, local memory, PMU, and timing generators are multiplexed sequentially between the test stations. The test stations contain the high-speed driver switches and comparators that are to be connected to the DUT. Any pin in the high-voltage test head has the ability to be programmed as any of the following:

- Clock channel
- Data input channel
- Detector output channel
- Bias or power supply channel
- Input/Output channel

3.7.1 Analog Interface

The RVS voltages are fanned out to the test head via the Analog Reference Module (ARM) where the DPS's go directly to two test stations where high speed driver switching between two voltage levels and output comparisons per pin are obtained within six inches of the DUT. Due to the design of the high-speed test stations, the analog buffers are not needed, as each pin electronic has its own self-contained buffer.

3.7.2 Pipelining

The operation of the pipeline in general is transparent to the user; timing relationships, strobe regions, mask and I/O changes etc., are not changed with changes in the test rate. Pipelining can also be accomplished via the controller. During functional testing, test patterns proceed synchronously through several stages of logic, such as local memory, formatter, pin electronics, strobe registers, etc. A sequencer controls the orderly flow of information through this pipeline. It controls startup and shutdown of tests and ensures proper test execution in various modes such as external sync mode and match mode.

3.8 High Speed Registers

There are several high speed registers in the high speed controller subgroup for control formatting and timing of local memory data input and

output to the DUT. These registers provide selection on a per-pin basis. The registers are:

- DA/DB
- MA/MB
- Enable IMASK
- I/O Mode
- I/O Mode 3
- Mux Mode
- XOR
- RZ
- Invert functional data
- ST
- TG1, 2, 3
- CRO
- C

Refer to figure 3-2 for the various waveforms created using the high speed registers.

3.8.1 DA/DB Registers

The DA/DB registers are I/O definition registers that allow for changing of input/output definition of any DUT pin "on-the-fly"; at the programmed functional test rate.

3.8.2 MA/MB Registers

The MA/MB registers are mask definition registers that allow the changing of "care-don't care" conditions on any DUT pin "on-the-fly". A "care" condition enables a defined output pin (defined by DA or DB or by I/O MODE) to be compared to the expected output state stored in local memory. A "don't care" condition disables a comparison of a DUT output with any expected value. These registers allow all outputs to be masked while the DUT is in an undefined state and then be switched on-the-fly to the specified input/output definition once the device has been initialized.

3.8.3 Enable IMASK Register

The Enable IMASK register allows the programmer to specify whether or not a pin in an input mode is an automatic "don't care". IMASK gives an alternate mask control saving local memory space since an I/O definition word also controls the mask and a corresponding mask definition words is not necessary for pins changing I/O mode.

3.8.4 I/O Mode Register

The I/O MODE allows pin W to have its I/O definition supplied by the F data (stored in local memory) of the pin adjacent to W independent of the DA/DB register definitions. For this operation, the system operates in a mode called I/O MODE. This allows completely independent changing of the I/O definition of up to 30 pins with each test pattern. The I/O mode for pin W can change within 50 ns of T0 (test cycle start) or after a programmed delay depending on the timing generator programmed to the adjacent controlling pin.

When the system runs in this mode and a pin W is defined as an input pin, fail data on the pin is automatically disabled; i.e., for each test pattern that defines the pin W as an input, the device output seen at this pin is a "don't care." Refer to figure 3-3 for I/O Mode pin patterns.

3.8.5 I/O Mode 3 Register

In I/O MODE 3, the input/output definition of a pin is identical to the functional data of an adjacent controlling pin, unlike the I/O mode where the controlling pin's functional data controls the I/O definition of three pins. Figure 3-3 shows which pins can be controlling pins and which can be controlled pins.

3.8.6 Mux Mode Register

In the MUX mode, the waveforms of two pins, X and Y, are ORed together and appear on pin X. Pins X and Y come in 32 pairs, as illustrated in figure 3-4.

Fig. 3-2 High Speed Registers Waveforms

	T0	T0	T0	T0	T0	T0	XOR	RZ	INV	* P.E.P.	COMMENTS
MDO F DATA	0	0	1	1	0						
TIME GEN (TG)											
EFFECTIVE WAVE FORM 1							0	0	0	-	Normal NRZ Mode Using T0
2							0	0	1	-	NRZ Mode for Inverted MDO DATA Using T0
3							0	0	0	NO	Normal NRZ Mode— Using TG
4							0	0	1	NO	NRZ Mode for Inverted MDO Data, Using TG
5							0	1	0	YES	Normal RZ Mode
6							0	1	1	YES	Return To One For Inverted MDO Data
7							0	1	1	YES	RZ for Inverted MDO Data (Disable RTOM)
8							1	0	0	NO	Logical Coincidence of MDO Data and TG
9							1	0	1	NO	Exclusive Or of MDO Data and TG

* P.E.P. = Pulse Exceeding Period Allowed

Fig. 3-3 I/O Mode and I/O Mode 3 Pin Patterns

CONTROLLING PIN	2	6	10	14	17	21	25	29	32	36	40	44	47	51	55	62	66	70	74	77	81	85	89	92	96	100	104	107	111	115
CONTROLLED PIN, IN I/O MODE (PIN W)	1	5	9	13	16	20	24	28	31	35	39	43	46	50	54	61	65	69	73	76	80	84	88	91	95	99	103	106	110	114
CONTROLLED PINS IN I/O MODE 3	1 3 4	5 7 8	9 11 12	13 15 19	16 18 23	20 22 27	24 26 27	28 30 34	31 33 38	35 37 42	39 41 45	43 45 49	46 48 49	50 52 53	54 56 57	61 63 64	65 67 68	69 71 72	73 75 79	76 78 79	80 82 83	84 86 87	88 90 94	91 93 98	95 97 98	99 101 102	103 105 109	106 108 113	110 112 117	114 116 117

Fig. 3-4 Mux Mode Pin Patterns

PIN X	1	2	3	4	5	6	7	8	31	32	33	34	35	36	37	38	61	62	63	64	65	66	67	68	91	92	93	94	95	96	97	98
PIN Y	16	17	18	19	20	21	22	23	46	47	48	49	50	51	52	53	76	77	78	79	80	81	82	83	106	107	108	109	110	111	112	113

This feature allows the Sentry to efficiently test devices that require multiplexing of the X-Y address lines. Address multiplexing means that both X and Y signals of an address appear on one line (or pin electronics) in a time-multiplexed fashion. For example, X0 = 1 appears on Pin 1 for the first 50 ns and, 20 ns later, the Y0 = 1 appears for 50 ns on the same pin. This means that in 120 ns, an address (X0 = 1, Y0 = 1 in this example) has been presented to the DUT on one single line.

3.8.7 XOR Register

The XOR register allows the data to an input pin to be exclusive ORed with TG data in order to apply worst-case waveforms to the DUT.

3.8.8 RZ Register

The RZ register defines whether an input pin operates in the RZ (return to zero) or NRZ (non-return to zero) mode.

3.8.9 Invert Functional Data Register

The invert functional data register allows functional data inversions in the RZ or NRZ mode on a per pin basis; thus, the waveshape is converted to return-to-one in the RZ mode.

3.8.10 ST Register

The ST register allows for selection of one or two comparator strobe timing generators for each 60-pin group. TG7 and TG8 are assigned to pins 1-60, while ATG7 and ATG8 are assigned to pins 61 through 120. A "one" in the register bit pattern causes TG8 or ATG8 to be used as a strobe on the respective pin. It is also possible to enable a double strobe

by the FACTOR statement "ENABLE DOUBLE STROBE." A "0" in the "SET ST binary pin pattern" connects both TG7 and TG8 strobes to that pin or, if the pin number is 61 to 120 ATG7 and ATG8 is connected. A "1" will cause TG8 or ATG8 to be connected to the pin.

3.8.11 TG Register

The TG1, 2, 3 registers allow for the selection of one of six timing generators for each 60 pins. TG1-TG6 are assigned to pins 1 through 60 while ATG1 through ATG6 are assigned to pins 61 through 120. The 'ORing' of timing generators TG1 and TG2 and the 'ORing' of ATG1-ATG2 is accomplished by the FACTOR statement: 'CGEN TG12 pin list'.

3.8.12 CRO Register

The CRO register controls the comparator relays on the pin electronics to allow isolation of the individual DUT pins for the tester.

3.8.13 C Register

The C register stores "FAIL" information based on comparisons between expected output values stored in local memory and the actual output value from the DUT. The register also shows which pin(s) "failed".

In addition to the above registers, the controller has several other registers that allow for selection of data/clock voltage levels, output comparison voltage levels, DPS select control, local memory address control, etc.

3.9 Local Memory Operation

Under normal functional test execution, functional testing proceeds by reading sequentially all local memory words from a start address S to a last address L. This may include looping back from L to address 0 (major loop), traversing this major loop N times. The test sequence may also include a minor loop between address J and K, which is traversed M times. Addresses S,J,K,L and counts M,N are programmable. Maximum count is 4096. Figure 3-5 shows the major and minor loops.

The tester will leave the normal test mode, generate an interrupt and become idle when address L is reached and major loop counter N is zero - this signals successful completion of a test - or when a test pattern fails and its address is larger than the address contained in the IF (ignore fail) register, signalling failure of a test.

Local memory may operate in one of several modes. Continuous loop mode is identical to normal test execution, except that testing will stay continuously in either the minor or the major loop when it encounters a loop. Loop counters will not be decremented. While in the loop, the mainframe can read or write words in local memory. This mode is terminated, under program control, by executing an ENABLE TEST MOMENTARY statement.

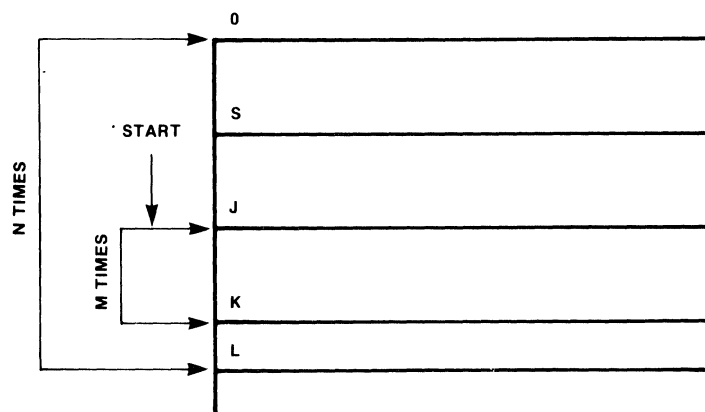
The momentary mode is enabled by the FACTOR "ENABLE TEST MOMENTARY" statement and causes the continuous mode to terminate. When the minor loop K address is next encountered, test execution will proceed to address K+1 rather than jump back to address J.

In the match mode, the tester stays continuously in the minor loop as long as each test generates a failure. On the first pass "match" the test sequence branches to address 0 and leaves the match mode. When in match mode, the test rate is constant throughout the entire functional test sequence; there is no Dummy Test Time. Minimum programmable period is 800 ns, TG7 (Delay + Width) period -600 ns. During the "search for match" only TG7 and ATG7 are enabled. TG8 and ATG8 are automatically disabled while searching for a match.

A sync pulse signal, which is generated whenever a specified statement or local memory location is executed, is supplied by a BNC connector at the front panel of the controller.

In the enable latches mode, once the mode is entered and the test enabled, functional testing will not be terminated, regardless of the number of failures that have occurred, until local memory reaches location L. The C register stores failures of all pins during the functional testing and will not be cleared during the functional testing. The C register may be cleared only if the DISABLE LATCH has been programmed and/or it is followed by a functional test and during the functional test no failure has occurred.

Fig. 3-5 Major/Minor Loops



The ENABLE TEST IFAIL statement initiates testing that will ignore all functional fails up through a local memory location as defined in the statement: SET IFAIL nnnnB; where nnnnB is the location in local memory or if SET IFAIL nnnnB COUNT is programmed, failures will be ignored up through the number of test cycles specified. The external sync mode allows the Sentry system to perform functional testing at a rate determined by the DUT. An external clock signal is brought into the time base via pin 1.

When external sync mode is programmed, the period must be in range zero, and until the first functional data pattern appears at the DUT, all timing generators will be disabled.

Logic levels of the external sync signal must be compatible with other outputs on the DUT, or level shifters are required at the performance board to provide the appropriate levels.

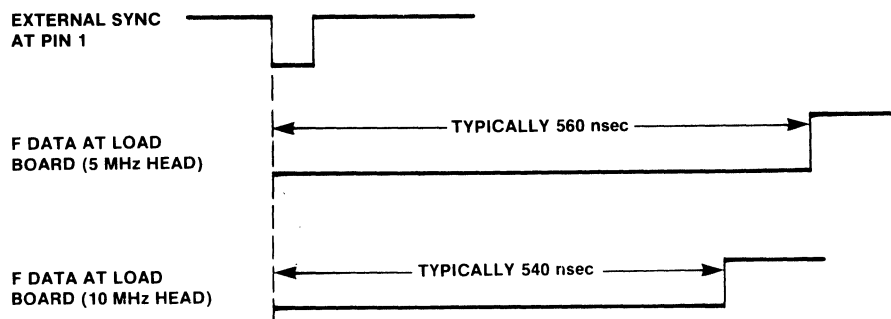
When match mode is not programmed, the minimum test period is 200 ns.

In external sync alternate mode, the timing generators are not disabled during the first functional test. This mode is for use with devices that give an external sync pulse at a known time, so that the period is not shorter than the delay or width of any timing generators programmed.

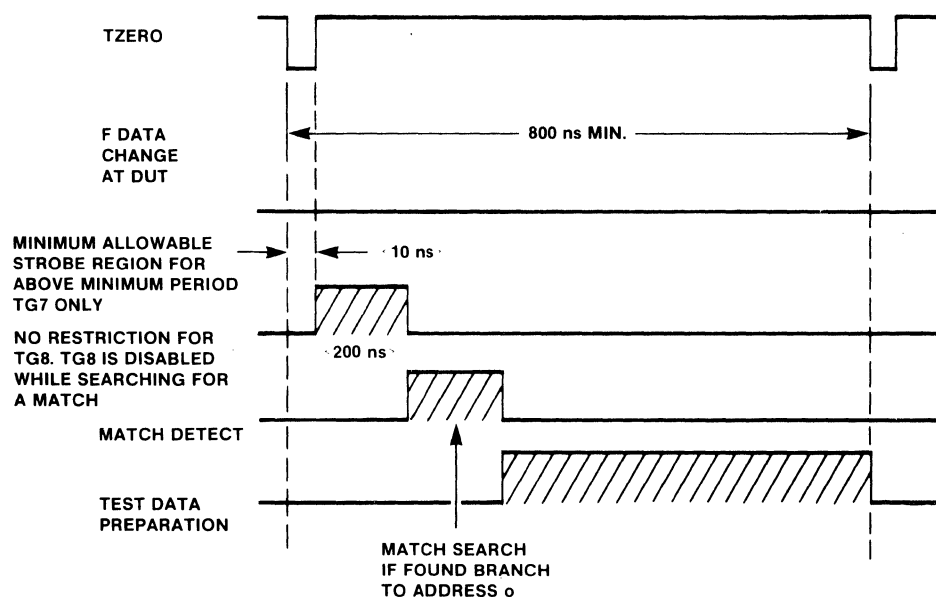
When the external sync circuit operates in match mode, the minimum test period is 800 ns. Test data arrives at the DUT typically 540 ns after the external sync signal. For Match mode, allowable programmed strobe time for Strobe 7 (delay + width) period -600 ns. Refer to figure 3-7 for mode timing diagrams.

Fig. 3-6 Mode Timing Diagrams

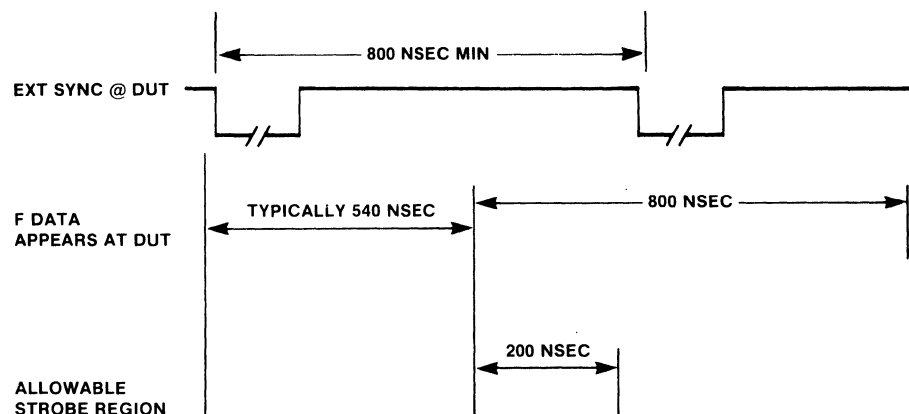
External Sync Timing



Normal Match Mode



External Sync Match Timing



In this mode, the tester stays continuously in the minor loop as long as each test generates a failure. On the first pass "match", the test sequence branches to address 0 and leaves the match mode. As long as the tester stays in a match mode, each test pattern is executed at a minimum rate of 800 ns.

The external sync match mode specifications are:

1. Minimum period = 800 ns
2. TG7 delay + width period - 600 ns
3. During "Search for Match", only TG7 and ATG7 are enabled
4. TG8 and ATG8 will be enabled immediately upon a match

3.10 Timing Generators

Sixteen timing generators are available and provide synchronization and timing for single or multiphase clock devices. These TG's also provide fail strobe and data timing for functional testing. If no timing generator is programmed, the start of test period pulse (T0) is used for data timing. TG1 through TG6 are used as inputs on pins 1 through 60 while ATG1 through ATG6 are used with pins 61 through 120. Refer to the specifications section for timing generator range information.

For those generators used as strobes, the strobe window equals the duration of its programmed width (10 ns to 5 ms). For high voltage and high speed test stations, the allowable strobe window is 10 ns from the leading edge of T0 to 10 ns from the completion of the period. The above times exclude the use of I/O switching.

In the double pulse in RZ mode if a pin is in the RZ mode, and it is connected to "TG12" via the FACTOR program, the logical OR of timing generators TG1 and TG2 will be used as the effective timing input to this pin. If the pin is in the upper ranks (pins 61 through 120) ATG1 and ATG2 will be used. Refer to figure 3-7 for double pulse Waveforms.

The accuracy of the double pulse mode is determined by pulse rise and fall at the DUT delayed by one ECL gate (2ns) with respect to a reference frame established by T0 and all other timing generators.

Pulse Exceeding Period is used in conjunction with TG1 through ATG6 only. If a pin is in the RZ mode it can be driven by a timing generator whose pulse delay + width exceeds one period (but is less than two periods). Refer to figure 3-8 for pulse exceeding period waveforms.

Fig. 3-7 Double Pulse in RZ Mode Waveforms

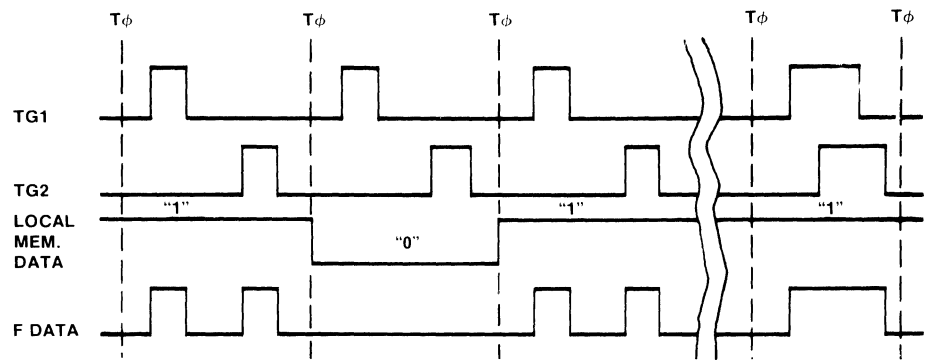
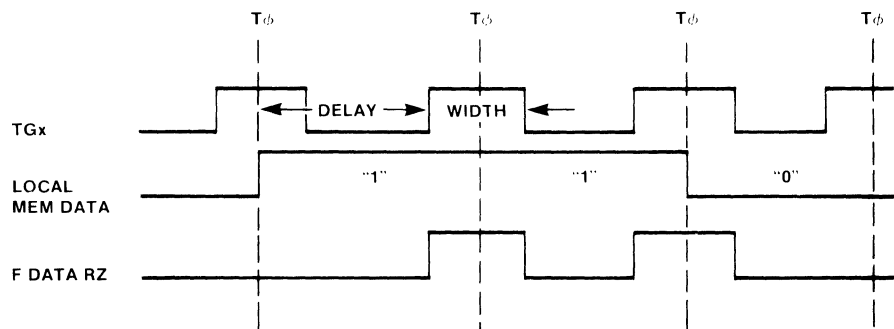


Fig. 3-8 Pulse Exceeding Period Waveforms



Test Stations

4.1 General Purpose Test Stations

Each test station contains a test head assembly with test head pin electronics. The pin electronics are the final link between the Sentry and the DUT. Pin electronics provide pin drivers and detector functions to each pin of the DUT and access to the DC testing and performance board. Refer to specifications section for pin electronics information.

The compact test head is designed for optimal device testing. Each pin electronics card is located in a "carousel" configuration that provides less than 6 inches of lead length to each DUT pin. The assembly will accommodate up to 60 pin cards to service up to 120 DUT pins. Each pin electronics card can function as data input driver, clock driver, device power supply, and data output comparator. Inputs can be switched to outputs within one data period; no pin board swaps are needed.

Test heads function with manual tests, wafer probers, or automatic device handler/chambers. This flexibility provides maximum device throughput with optimum data correlation between wafer test and final test.

4.1.1 Pin Electronics (5 MHz or 10 MHz)

The pin electronics circuitry is designed to function in any one of five possible modes completely under program control to provide the user a system that can be easily programmed to a specific application:

- Data mode
- Clock mode
- Output mode
- Input/Output mode
- Power supply mode

Functionally the pin electronics receives two types of digital data. Low speed control data that establishes the modes of operation and high speed functional data that establishes conditions to be met in that particular mode.

In addition to the digital data, the pin electronics receives two types of analog data from the reference voltage supplies. The first type (E0, E1) establishes the "one" and "zero" logic levels that are to be forced in the clock and data modes. The second (S1, S0) establishes the voltage levels for sensing at the detector.

The pin electronics provides a forcing voltage to the DUT and/or compares an output from the DUT with S1 or S0 reference and sends digital data that represents the results of the comparison back to the Pin Control II logic to be processed.

The pin electronics also provides a low impedance path to the pin for parametric measurements by the PMU.

A functional block diagram of pin electronics inputs and outputs is presented in Figure 4-1. The specifications section gives the detailed information concerning the high voltage pin electronics.

The data driver and clock modes provide the digital input and clock forcing voltage and timing for the DUT.

The output mode (comparator) provides the comparison information for the output from the DUT.

Using an additional local memory channel, one of two mask registers can be gated with the comparator with each functional test. If the channel contains a 0, then mask register MA will be used, and conversely, if it is a 1, mask register MB will then be used. This allows up to two masks to be used for any given data channel and mask selection can change at the beginning of each test period.

One or two strobe patterns may be selected by each pin. The strobe patterns have programmable width and delay. Also the strobes may be ORed together to create a composite strobe pattern. Failures may be detected any time during the strobe window.

In order to select a double strobe, Strobe B must be selected; therefore, some pins may be Strobe A and others the composite strobe pattern. Figure 4-2 shows the strobe patterns. Figure 4-3 shows allowable strobe regions.

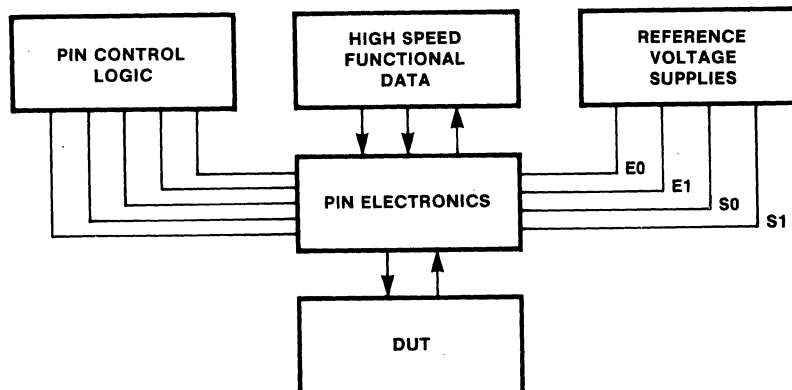
The power supply mode uses the driver as a supply thus allowing the use of the DPS reference supplies as bias (100 mA steady state). The four available reference supplies are Tester Common (TCOM), DPS1, DPS2, and DPS3.

The standard DPS supplies are brought to the test head and available at the performance board for connection to the DUT when currents up to 1 amp or large positive voltage are required. Amplitudes of +51V to -29V relative to Tester Common (TCOM) are possible with this connection.

NOTE

The DPS supply output is offset from TCOM by +11V when used directly at the test head (not via the pin electronics)

Fig. 4-1 Functional Block Diagram of Pin Electronics Inputs and Outputs



Reference select logic is provided by four data drivers, E0/E1, EB0/EB1; two comparators S1/S0 four clock drivers EA0/EA1, EC0/EC1 and four bias supplies/ground, DPS1, DPS2, DPS3, and TCOM.

NOTE

A data driver may be used as a clock driver by definition of the RZ register. A clock pin may conversely be changed into a data pin by definition of the RZ register.

Fig. 4-2 Strobe Patterns

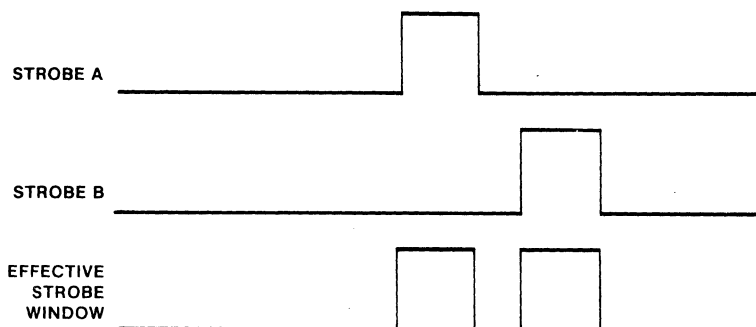
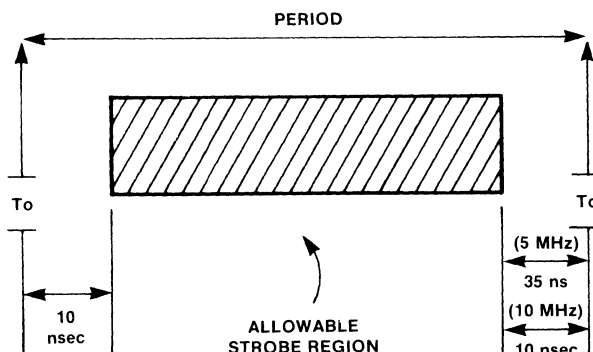


Fig. 4-3 Allowable Strobe Region



Provisions are made to allow switching (via a spare local memory channel) from an input to an output or vice versa within 50 nsec, at the beginning of the cycle, for data pins only.

4.2 High Speed Test Station

Development, characterization and testing of such high speed technologies as ECL, I^2L , NMOS, and Schottky TTL have created a need for a test system that is capable of testing VLSI with fast accurate pulses at low voltage excursions. The high speed test station is available to meet these needs. Refer to specifications section for detailed high speed test station information.

Timing characterization with 160 pico second resolution can now be performed using pulse widths as narrow as 10 ns. Adjustable skew on the

data and clock drivers as well as skew adjustments on the output comparators allow the Sentry to present a true picture of device timing relationships.

A special clock driver pin electronics has been developed in addition to a new data driver. The clock driver allows voltage excursions of 17V. (-1V to +16V) while the data driver is capable of -1 to +6V swings. The individual pin electronic board may consist of 2 data drivers or one clock driver and one data driver, the clock driver representing the odd numbered pin in the test station. Up to eight clock driver pin electronics may be used in the high speed test station in any odd numbered position except pin 1.

NOTE

Fairchild recommends the following pin locations 15, 25, 45, 55.

The pin electronics receive two types of digital data consisting of low-speed control data to establish the mode of operation and high speed functional data that establishes conditions to be met in that mode.

The analog voltages are made up of driver voltages which are used to establish the '0' and '1' level to the device under test and reference levels which are used by the level detectors to sense data from the DUT. The output from the DUT is sent back to the Pin Control II logic for processing after it has been compared with the reference levels and converted to ECL levels.

Each pin electronics also serves as a low-impedance path to the DUT to allow the PMU to perform complete parametric measurements on any DUT pin. These measurements can be made while the DUT is functionally active to permit power average readings to be made. Refer to figures 4-4 through 4-9 for graphic representations of high-speed test stations specifications.

Using an additional local memory channel, one of two mask registers can be gated with the comparator with each functional test. If the channel contains a 0, then mask register MA will be used, and conversely, if it is a 1, mask register MB will then be used. This allows up to two masks to be used for any given data channel and mask selection can change at the beginning of each test period.

One or two strobe patterns may be selected by each pin. The strobe patterns have programmable width and delay. Also the strobes may be ORed together to create a composite strobe pattern. Failures may be detected any time during the strobe window.

In order to select a double strobe, Strobe B must be selected; therefore some pins may be Strobe A and others are composite strobe pattern.

The standard device power supplies are brought to the test head and are available at the performance board for connection to the DUT.

Reference select logic is accomplished by:

- Four data drivers - E0/E1, EA0/EA1.
- Four comparators S0/S1, SA/SA1.
- Two clock drivers EA0/EA1.

The Sentry is capable of switching the data driver from an input driver to an output comparator and vice versa at real time by use of a spare local memory channel. This switching is accomplished within 10 nsec of T0.

All comparator relays may be opened by software control to isolate DUT output pins.

Fig. 4-4 Specifications for HSPE Definition of Terms

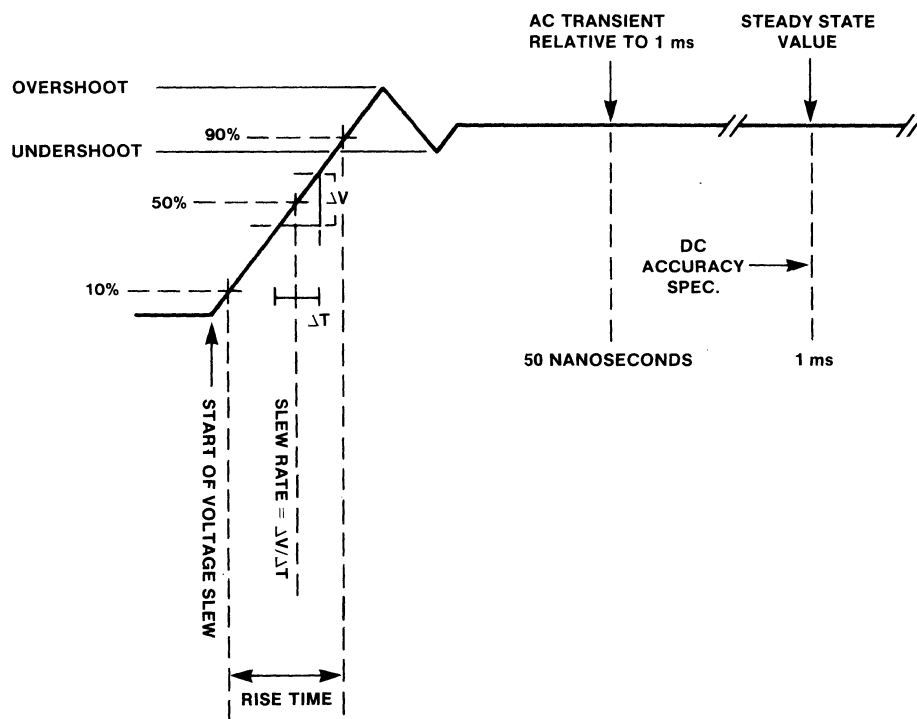


Fig. 4-5 Rise/Fall Time Linearity

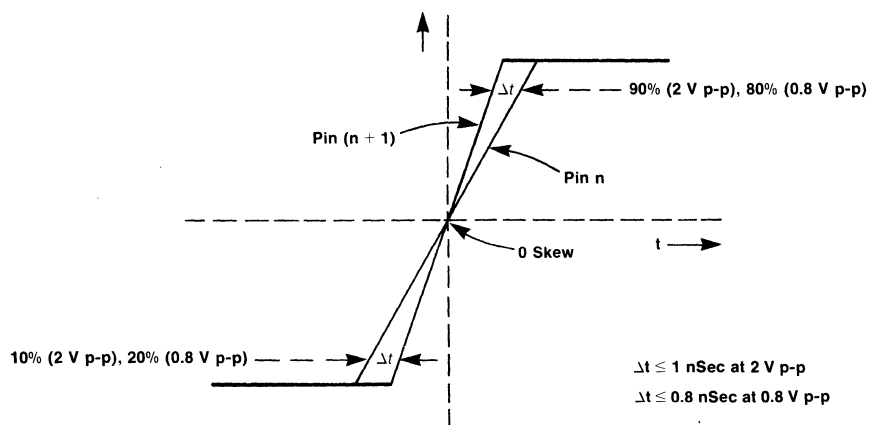


Fig. 4-7 Comparator Linearity

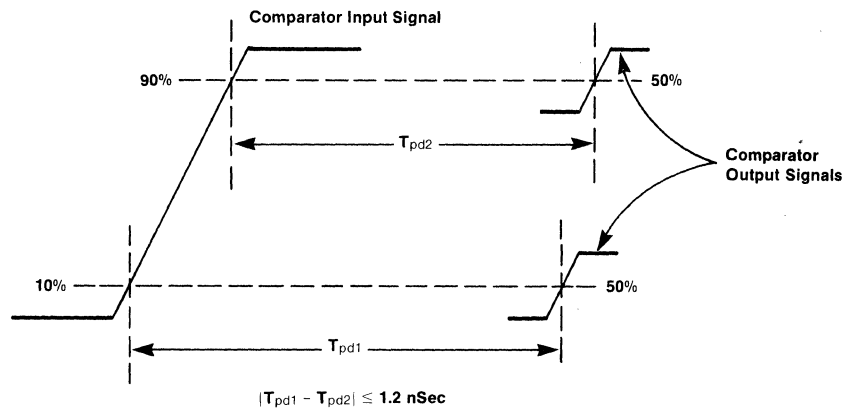


Fig. 4-8 Change in Propagation Time with Change in Input Overdrive

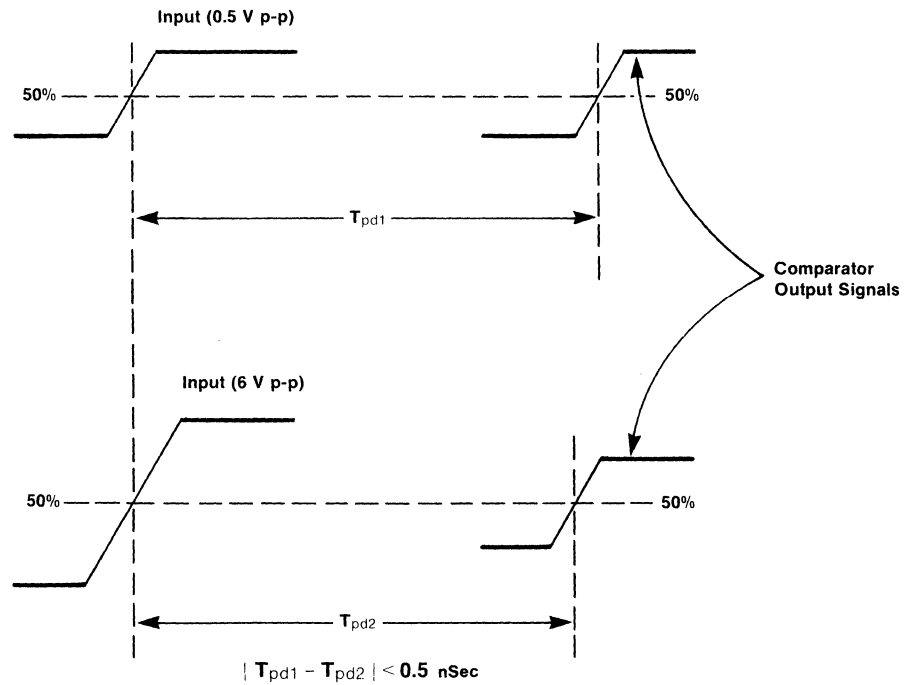
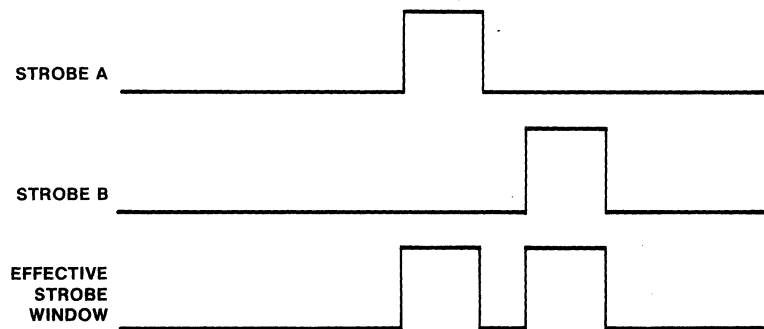


Fig. 4-9 Strobe Patterns



4.3 28V High Voltage Test Stations

The 28 volt feature increases the voltage output of the high voltage pin electronics to +6V to -22 V at frequencies below 5 MHz thus further increasing the flexibility of the Sentry test system.

4.4 Interfacing Test Head

It is possible to interface the test head electronics to one of three types of handlers.

- Wafer Prober - up to 120 pins with provision for external components and pin routing.
- Manual or Automatic Package Handler
- Environmental Automatic Package Handler

4.5 Performance Board Group

There are two performance board types available with the Sentry VIII for interfacing the test station to the DUT.

Passive component may be connected to a device via the performance board to provide a load on the output. For certain device types, with open collectors, for example, a load is required for proper logic functioning. Active components may also be used for special pulse shaping or logically combining tester signals or other like purposes. Typically, passive or active components are connected to the relay side of the pin rather than the force side. The components may then be connected or disconnected under program control.

The solid center performance board is used for manual insertion testing (see figure 4-10). Typically this board is used to mount device sockets that are not of the Textool type. The performance board artwork is designed to accommodate one relay for each pin of the tester. Individual control lines for each relay are provided which enable the user to load the device under program control.

A solid center performance board is also used for Textool sockets. This board has the same functions as the solid center board with the addition of a pin pattern design that accommodates 14, 16, 18, 24, and 40 pin Textool sockets. Note: Textool is a trademark for test sockets.

A special TVFY performance board (figure 4-11) is used in conjunction with the TVFY software diagnostic program. This allows the user to thoroughly test each test station.

The 60 pin to 120 pin performance board adaptor (figure 4-12) is available to insure the compatibility between the 60 pin versions of the Sentry V and Sentry VII test systems and the Sentry VIII test systems. This performance board interfaces between the pin electronics and the existing performance board. This means that no rework is necessary for implementing current test programs and performance boards.

4.6 Test Station Control Panel

Each test station has sufficient controls/indicators to display test information and manually control test information and manually control test execution. Refer to figure 4-13.

Fig. 4-10 Solid Center Performance Board

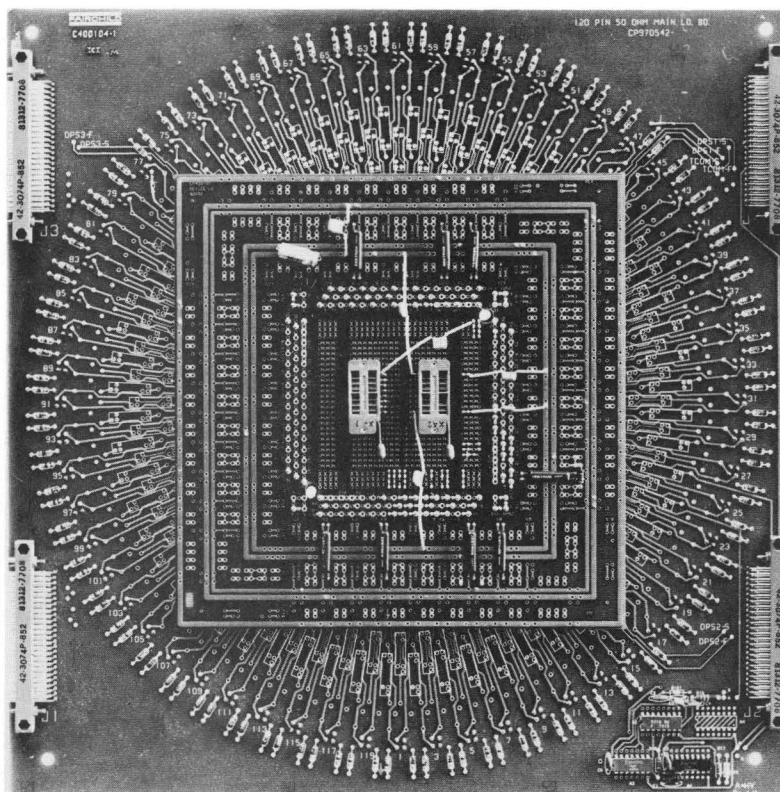


Fig. 4-11 TVFY Performance Board

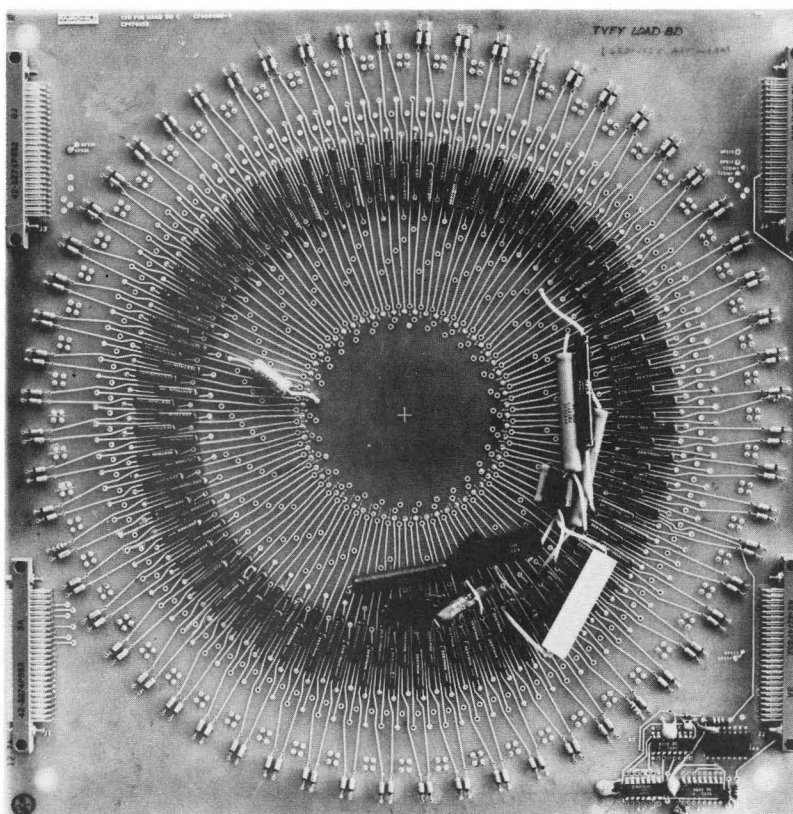


Fig. 4-12 Performance Board Adapter

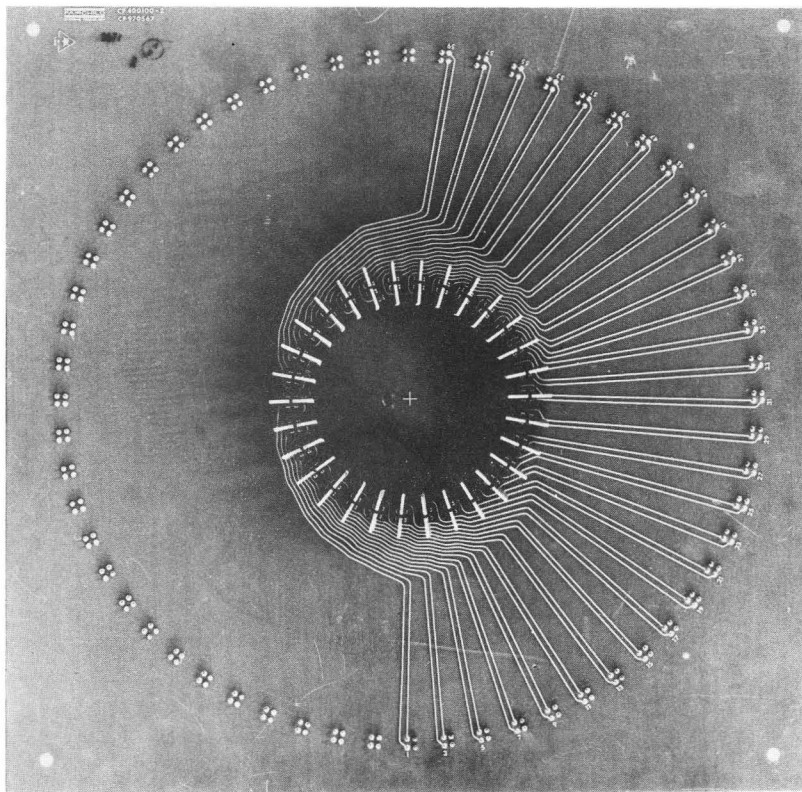
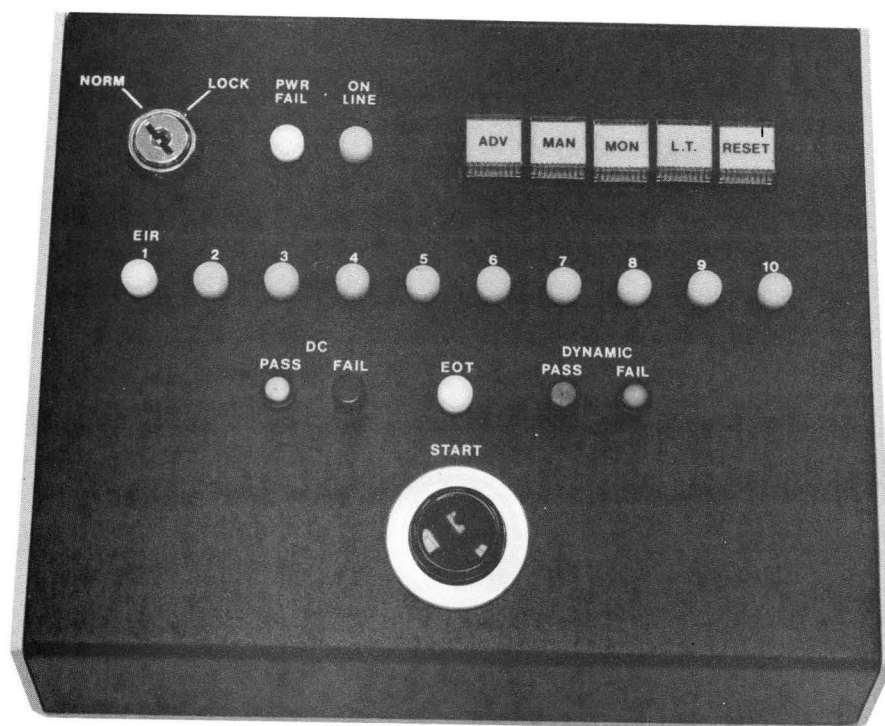


Fig. 4-13 Test Station Control Panel



SPM/PPM

This section briefly describes the functions of the SPM and PPM options. Figure 5-1 shows a block diagram of the SPM and PPM options.

5.1 Sequence Processor and Pattern Processor Options

The Sequence Processor meets a large number of key requirements for testing modern complex devices and anticipates the needs for testing microprocessors, communications and other devices which are evolving. The Sentry Sequence Processor provides enhanced capabilities for testing devices that require flexible input/output control of individual pins, long functional test patterns and sequences, high speed and absence of data breaks.

The ability to execute a large number of commands at full 10 MHz data rate reduces the amount of test time and hence the cost of high speed memory required. This efficiency of testing also greatly eases the quantity and cost of programming.

Local memory is already capable of operating at up to a 10 MHz rate and of storing 4096 120-bit patterns of functional test-and-compare data. The sequence processor augments the Sentry high-speed local memory by adding a control word to the local memory functional data words for memory address control, I/O control, and mask control.

The large number of sequence processor options for real-time control of I/O definition, masking and timing eases test generation. Devices having wide I/O buses and variable I/O groups may be handled as easily as devices having dedicated pin assignments.

The sequence processor is a processor with a high-speed TTL microcode store. The microcode store contains up to 4096 words of 16-bit microcode, and the processor has two main sections: the address control section and the timing section.

The address control and timing sections of the sequence processor fetch and interpret the microcode commands from local memory at the same time as a 120-pin wide field of functional and compare data is fetched from the local memory's functional data store.

5.1.1 SPM Microcode Commands to Modify Test Pattern Sequence

Microcode commands allow efficient re-use and modification of data already in local memory. Ordinarily, functional testing proceeds by reading sequentially all local memory words from a start address to a last address. This sequential test execution may be altered by the following microcode commands:

- **Clock Burst.** A clock burst is basically a loop confined to one pattern at one memory location. This pattern is repeated a specified number of times. If the DUT requires repetitive data in its test sequence, a clock burst command is used. Each functional pattern can be repeated up to 4096 times, and each clock burst is variable in count from one clock burst command to the next.
- **Subroutine Call.** Allows branching out of sequential order to a subroutine.
- **Subroutine Definition and Loop Count.** Use of the subroutine loop is largely for execution of often-used sequences. Looping on a group of patterns is allowed in a subroutine loop; the loop will be traversed until the loop count is exhausted before the subroutine return is taken. A subroutine loop can be called from any portion of local memory and can contain any other patterns or commands, including other subroutine calls. Subroutines may call subroutines and nest up to 16 levels deep.
- **LSUBR SUB NORMAL n; SET F;** defines a subroutine called SUB and says it is to be repeated n times; n can be 1 to 4096. (Normal indicates that this is a normal test, without match mode, continuous loop mode, sync mode, or other modifications.) The return address and loop count are stored in hardware push down stacks; thus, after completion of the requested number of subroutine loops, the tester returns to the next pattern in the sequence it was running before it branched to the subroutine.
- **Unconditional Jump.** Unconditional jumps are a way of linking sequences in local memory. Because the jump-to location may be changed from the system CPU, the entire sequence may be reordered with one statement. In addition, jumps may be inserted under keyboard controls to allow looping for debug purposes.

5.1.2 SPM Microcode Commands to Modify Registers

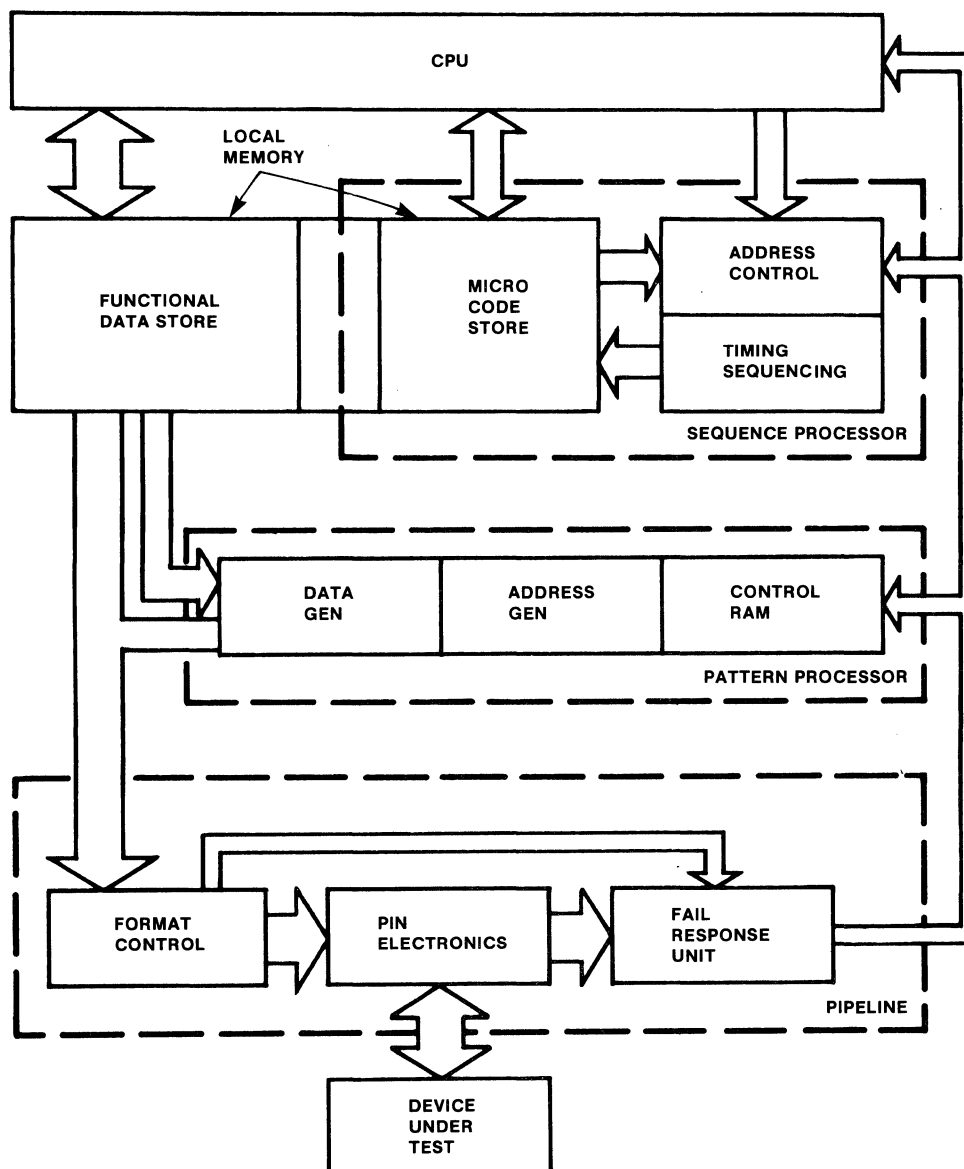
Register load commands are part of the sequence processor for on-the-fly reassignment of pin I/O definitions, care/don't care masking, and pin timing.

There are two I/O definition registers, DA and DB, which allow for changing the Input/Output definition of any DUT pin. Ordinarily, DA and DB are preloaded by the system computer and selected on-the-fly by two extra control channels in local memory.

With the sequence processor, these registers may be controlled by using the function data field of local memory to load the I/O registers in response to a microcode command. In addition to selecting DA or DB on-the-fly, the program can modify DA or DB at a 10 MHz rate (subject to cycle steal).

Care/don't care masking registers, MA and MB, can also be modified on-the-fly with the microcode command: LSET MA/MB (subject to cycle steal).

Fig. 5-1 Sequence Processor and Pattern Processor with Local Memory & Pipeline



Waveform control is controlled by the commands LSET XOR, LSET RZ, and LSET STROBE. They change the exclusive-OR, return-to-zero, and strobe select registers on-the-fly. Because these functions are not pipelined, some care must be exercised in usage.

Pin timing is handled by the command LCGEN TGn. This allows reassignment of timing generators to pins on-the-fly. As with LSET XOR, this function is not pipelined and special rules apply.

5.1.3 SPM Microcode Commands to Modify Testing

There are occasions when local memory data must be changed before it can be re-used. For this purpose, the processor uses its local memory alteration commands in conjunction with the system's invert functional data register. This invert register can invert functional data on a pin-by-pin basis. The invert register can be set on-the-fly by LSET

commands. Changes to the invert register can be done simultaneously with a subroutine call, thus causing the subroutine to produce different patterns each time it's called. In fact, the invert register may have a subroutine call (LCALL) attached to it.

5.1.4 SPM Microcode Commands to Modify Local Memory Continuous Loop Mode

There are two sequence processor instructions that put the system in a continuous loop; either instruction will inhibit all fails. LSUBR SUB CONTIN n; defines the start address of the continuous subroutine SUB. When the loop count n is exhausted and ENABLE TEST MOMENT has been executed, address control returns to the calling address plus one. With SET FC CONTIN, the F pattern is repeated continuously until the execution of ENABLE TEST MOMENT, which will then advance the local memory to the current address plus one.

While in the loop, the mainframe can write words in local memory; continuous loop mode allows alteration of local memory from the CPU memory without stopping local memory. When continuous loop mode is entered, a hardware function causes the start-up of the DMA channel from CPU memory, and alteration of local memory proceeds. This form of local memory alteration causes no timing disturbance in the test since testing is going on continuously during alteration.

Continuous Loop Mode is also beneficial to the user doing manual analysis.

5.1.5 SPM Microcode Commands to Modify Conditional Jump (MATCH) Mode

A form of conditional branch or branch on match is appropriate when the device being tested cannot be initialized and legitimate testing can begin only when a particular output pattern or group of patterns appears. For example, the leading or trailing edge of some signal or a particular bit sequence must be found before testing can begin. In match mode, testing continues until the desired condition is found.

A match is defined as a test or a series of tests the result of which matches an expected pattern.

With the sequence processor, matching may be done in any loop, either clock burst or subroutine. Thus, it is possible to test devices that require

In any type of match search, if the match does not occur within the programmed loop count of the burst or subroutine, a hardware fail interrupt will be forced since the device is presumed inoperative.

Regular Match and Alternate Match. LSUBR sub MATCH n defines the start of a match subroutine. A match within the subroutine will cause a branch to the calling address plus one. If the expected pattern or patterns cannot be matched within the loop count n, the local memory controller will cause a hardware trip and set the fail flag.

Set FC MATCH n seeks a match by repeating the same F pattern to the DUT; n serves as a burst count beyond which the test sequence is terminated and fail interrupt is set. Upon a successful match, local memory address will advance to the next location.

With regular match mode, the test rate can be programmed up to 1.25 MHz. Alternate match mode can be done at the maximum speed of the machine (10 MHz) except that branching always lags the successful match by six extra cycles.

Sequential Match. A sequential match is defined by a desired pass/fail sequence. The sequence processor's match-to-a-sequence capability allows it to find leading or trailing edges without ambiguity and to find pulses of specified widths. SET Q xxxxxxxxxxxx is used in conjunction with the ENABLE TEST MATCH/AMATCH statement to search for a sequential match on a pass/fail pattern. The "search pins" enabled are defined by one of the mask registers. The pass/fail data is transferred after each test from the C register into the C-save register. When a match is found, the contents of C-save match the contents of the Q register and control is passed to the subroutine calling address plus one or the FC+1. The sequential match mode is reset when a sequential match occurs or by a SET Q 0.

Ignore Fail by Count and Datalog. To create a full picture of device characteristics and failures, the sequence processor has ignore failure commands, commands that allow testing to continue after a failure. The count of failures to be datalogged can be up to 8,388,609.

DATALOG FCT m COUNT STATxx enables the datalogger to log m failures until the test ends. Use of the DATALOGGER and the FACTOR command SET IFAIL n together allows the user to specify whether datalogging is to begin at a specific memory location, at a test sequence start location, after a specific number of local memory tests, or at the first local memory test.

Failures can be logged by local memory location number or by test sequence number. Because of the numerous opportunities to reuse local memory locations, the capture of fail information must receive special treatment; a failure at a particular memory location may not be of significance in itself. Therefore, provision has been made to log not only the memory location of a fail, but also the total test count since the initiation of the functional sequence. This feature allows the failure always to be pinpointed, even though it is deep within a complex sequence.

5.2 Sequence Processor Manual Analysis

Manual analysis is a software program that enhances the user's ability to debug test plans with maximum efficiency. Under manual analysis, the user has the ability to read and write the following SPM registers:

- Start Register (SA)
- Return Address Register (RA)
- Clock Burst Clock (FC)
- Loop Count Stack (LCS)
- Stack Address (STAM)
- Ignore Fail Register #2 (IF2)

5.3 Sequence Processor Diagnostic (SPDG)

The diagnostic package supplied with each sequence processor module is a system of assembly language and FACTOR programs to test all functions of the SPM. SPDG assumes that TVFY, the Sentry system diagnostic, has been successfully run.

SPDG is divided into nine tests. The operator may pause or loop on each or any detected error inside a test. At the completion of each test, a message is output to inform the operator whether the test passed or failed.

The first test checks for correct local memory terminations.

The second test contains six subtests to verify individual local memory commands; each of these subtests is run in both internal and external clock mode.

The third test, the clock burst test, causes local memory to execute a SET FC command and verifies the time to execute the command.

The fourth test causes the local memory processor to execute a program that nests 16 levels deep and exits on an error. When it exits, the contents of the stack, loop counter, and stack pointer are verified. If the results are correct, all ones, all zeroes, and two checkerboard patterns are flushed through the stack and loop stack.

The fifth test verifies loop entry and exit timing by causing local memory to execute a program that nests 16 levels and terminates normally. When a program terminates, a timer value is checked.

The sixth test verifies escape from continuous loop mode via the enable test momentary command. The test also verifies escape from a continuous clock burst.

The seventh test modifies local memory while the local memory processor is executing a continuous loop and verifies the contents of local memory upon termination.

The eighth test causes a series of clock burst commands to be executed in match mode with only the last one causing a match. At termination, the time and termination address are checked. A match loop is executed next and the termination address checked. Finally, a sequential match is checked in normal and alternate mode. This test is run in internal sync mode and then in external sync mode.

The ninth test attempts to force errors by executing sequences of commands in XOR, MUX, IMASK, and AMATCH modes. Match mode is used with clock bursts, match loops, and sequential match loops. Inside these loops, the masks and I/O pin definitions are changed.

5.4 Pattern Processor Module (PPM)

The Sentry Pattern Processor was developed for evaluating large-scale memory chips with complex cell patterns that must be fully verified and where each individual cell must be verified.

The pattern processor with the Sentry enables a memory device (RAM, ROM, shift register) to undergo pattern testing of its memory matrix, parametric testing of its DC characteristics, and additional functional testing from local memory all in one test sequence.

The pattern processor is a microprocessor that has three high-speed ECL RAMs and six X-Y-coordinate registers. It works in conjunction with the first 60 pins of the Sentry local memory and fits into the testing pipeline.

The user controls and directs the pattern processor with microprograms. Each microprogram is accessed and executed from a FACTOR program (much like subroutines are called, except microprograms execute faster and more efficiently). Because the microprograms are separate name modules, the same microprogram can be called from several FACTOR programs for efficient use of system resources.

Even though microprograms are initially stored on the disc, they are accessible quickly because up to ten microprogram modules may be stored in the FST-2 memory and quickly transferred using DMA to the pattern processor when needed. Refer to table 5-8 at end of this section for PPM pin assignment.

The user writes microprograms with three types of programming instructions:

- Assembler directives
- Definition instructions
- Microinstructions

5.4.1 PPM Assembler Directives

Assembler directives give the pattern processor assembler information for converting a source microprogram into a microprocessor executable program. Table 5-1 lists the PPA directives and mnemonics

5.4.2 PPM Definition Instructions

Definition instructions are used to initialize the registers that are used to perform pattern testing; the instructions provide the set-up information necessary for execution of the microprogram. Table 5-2 lists the definition instructions and mnemonics.

The pattern processor has ten registers for X and Y. Three holding registers are for the initial X- and Y-values, (three values each). Three delta registers contain the amount by which X and Y are to be incremented or decremented. One limit register holds the maximum X and Y values, the values that define the size of the memory under test. Three index registers are the working registers for X and Y values.

5.4.3 PPM Microinstructions

There are two types of microinstructions: address generation and data generation. The pattern processor's high speed ECL control RAM stores these microinstructions, and each 44-bit word in the control RAM is either an address generator word or a data generator word. Figure 5-3 shows the major attributes of a memory test pattern.

The microword eliminates pattern generation overhead, and the result is decreased test time and increased throughput, fewer program steps, and lower programming costs, and pattern generation flexibility.

Table 5-1 PPM PPA Directives

Directive	Mnemonic
Define an address generator block	AGEN
Define a data generator block	DGEN
Define the end of program file	END
Define the start of a program module	PGMID

Table 5-2 PPM Definition Instructions

Instruction	Mnemonic
Load Hold Register pair	HLDm (Xm), (Ym)
Load Delta Register pair	DELM (XM), (Ym)
Load Maximum Register	MAX (SMAX), (YMAX)
Load Refresh Count Register	RFC integer
Load Chip Select	CSEL integer
Load Storage Address Register	ORG integer
Load Shift Data Register	SHFD integer
Load Data RAM	DATA n1, n2, n3, n4
Load Topological RAM	TOPO (X), (y)
Load Msk for X coordinate	MASKXinteger
Load Mask for Y coordinate	MASKYinteger
Disable/Enable Data Extension	DEX 0/1

The control RAM is 64 words long, and microprograms big enough to handle today's memories take only half of the microprogram space available in the control RAM. The PPM can handle a memory up to 16 8X and Y address lines, 18 data-in lines, 18 data-out lines, a read control, a write control, 3 power supplies, and four chip-select lines at a 100 ns cycle time (10 MHz test rate).

Address generation instructions define and control the execution of a sequence pattern. They update the coordinate registers, execute read-write operations on the memory under test, compare coordinate registers, and control the execution sequence by branching. Refer to figure 5-3 for address generation registers in PPM.

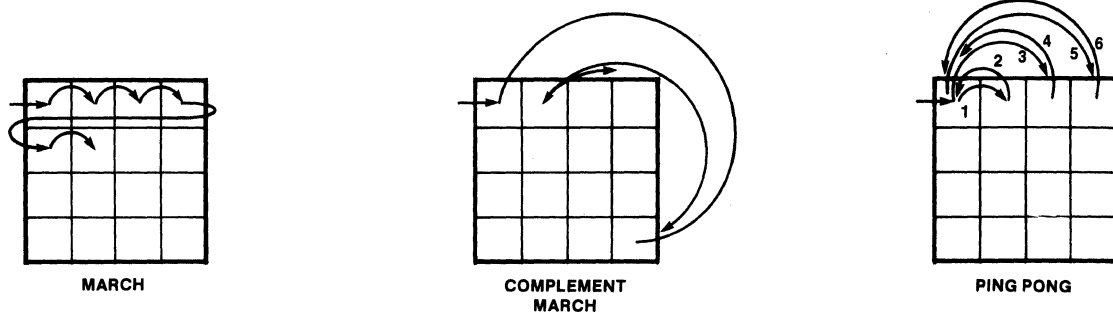
In a microword coded to generate an address, one microword can perform 20 operations simultaneously: specifying a branch condition, a branch address, read, or write; enabling or disabling chip select; inverting data; incrementing, decrementing, or loading any one or all of the three pairs of X and Y registers; and determining which of the three pairs of X and Y registers is to be applied to the DUT and also to be used as the address from which the data in and data out are generated.

Address generation flexibility comes, in part, from the pattern processor's six registers for storing X and Y coordinate values. The independence of the set of X-coordinates and the set of Y-coordinates from each other greatly simplifies programming array-oriented patterns, and the three pairs of X and Y coordinate working registers greatly increase the addressing combinations in a pattern-test sequence.

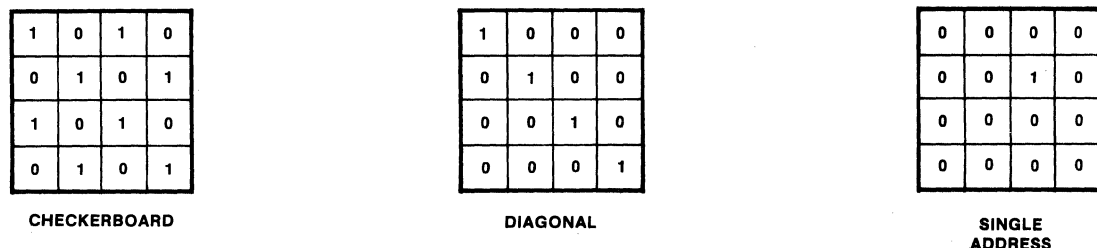
Patterns like the "butterfly" are easily implemented on the pattern processor because of the independent X and Y addressing. In the butterfly, each test cell is surrounded by a spiral address sequence.

Fig. 5-2 Major Attributes of a Memory Test Pattern

ADDRESS SEQUENCE



DATA PATTERN



After traversing all X and Y address sequences, the test cell is moved typically along a diagonal. Refer to figure 5-4 for butterfly pattern of first 16 address transistors.

The address generator instructions listed in Table 5-3 directly control the X-Y register values.

Address generation flexibility can also be seen clearly in the read-write operations. The read/write instructions are listed in table 5-4.

For instance, W writes a data pattern into a cell of the memory-under-test. The location of this cell is indicated by the coordinate values (Xm, Yn) in the working registers. WI writes the binary complement of a data pattern into the cell indicated by the coordinate values in the working

Table 5-3 PPM Address Generation Instructions

Instruction	Mnemonic
Increment index register by Delta value	INC Xm INC Ym
Decrement index register by delta value	DEC Xm DEC Ym
Load index register with holding value	L Xm L Ym

Table 5-4 PPM READ/WRITE Instructions

Instructions	Mnemonic
Write	W ±Xm, ±Yn
Write Invert	WI ±Xm, ±Yn
Read	R ±Xm, ±Yn
Read-Modify-Write	RW ±Xm, ±Yn
Read-Modify-Write Invert	RWI ±Xm, ±Yn
Operate	OP ±Xm, ±Yn
Operate Invert	OPI ±Xm, ±Yn

registers. Not only can users write the binary complement of the data pattern, they can also write into the location defined by the binary complement of the X and Y values (Xm, Yn) in the working registers.

Split-cycle timing allows intermixed read, write, and read-modify-write cycles without timing compromise. Split-cycle timing lets the system user test read cycles to stringent limits. ENABLE SPLIT is a FACTOR statement that allows tests to be executed at the APERIOD (alternate test rate) during the read cycle. This alternate test rate can be 100 ns to 40 ns. The alternate timing generator (ATG4) is used with the alternate test rate during non-write cycles.

The capability to split test rate and pulse width between read and write test cycles - to use different values - enables the user to test memories with different read and write cycle times without tying the test to the longer cycle. Moreover, cycle splitting is done on-the-fly.

Fig. 5-3 Address Generation Registers in the Pattern Processor

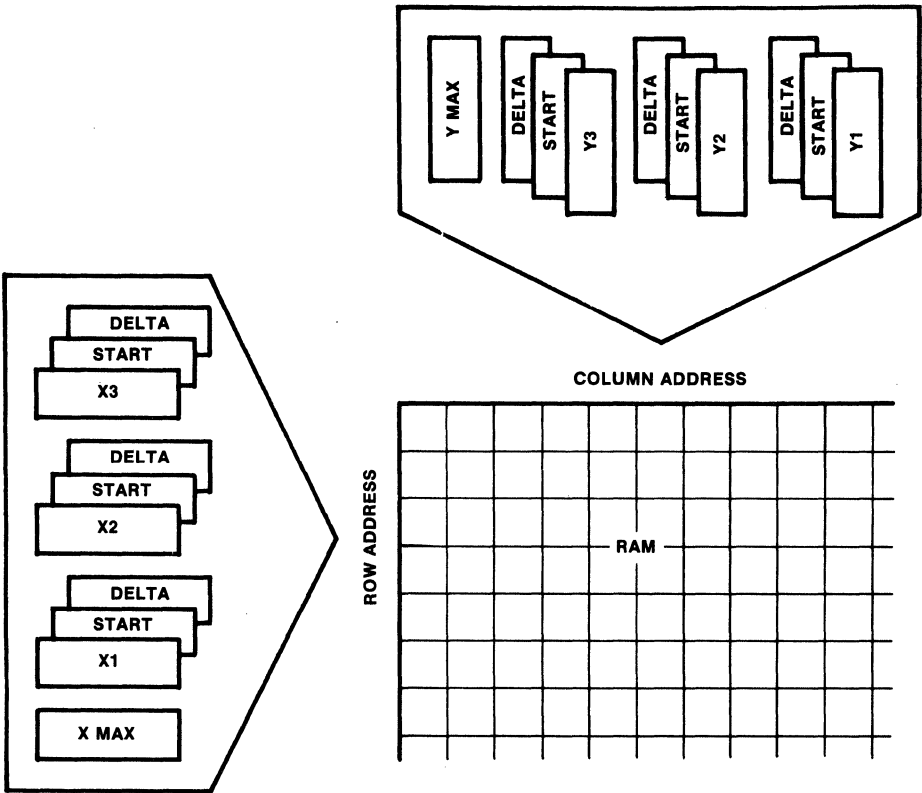
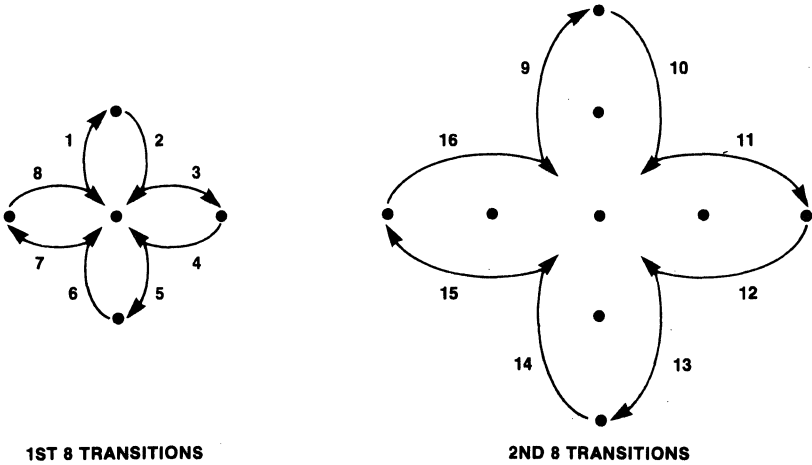


Fig. 5-4 “Butterfly” Pattern, Showing the First 16 Address Transitions



In conjunction with register changing and binary complement capabilities, address generator words are also capable of comparisons, branching, chip selection, and programmable refresh. Table 5-5 lists the compare and chip selections and refresh instructions.

CE and CG compare the chips of one register to another. If equal, CE sets a hardware indicator to "true". If the first is greater than the second, CG sets a hardware indicator to "true". These "trues" could trigger a branch to elsewhere in the program.

CHPS enables or disables chip selection; when enabled, memory testing is confined to memory devices with the proper chip select combination.

Asynchronous/Synchronous Refresh Timing. The size of the refresh interval is set by a definition instruction as a multiple of 10 us and can be set from 10 us to 650 ms. The refresh counter counts asynchronously with the test rate. The pattern program proceeds in its own sequence until a refresh interrupt occurs, at which time a programmed refresh pattern sequence may be executed. RFEN enables or disables the programmable refresh interrupt. When enabled, refresh is allowed at any point in the pattern. A synchronous refresh may be simply programmed and executed at the desired time by using a subroutine call.

The second RAM in the pattern processor is the 256-word-by-16-bit topological RAM. For memories where device pin order and array location aren't one-for-one, the topological RAM stores address scrambling data to make the desired test sequences; the topological RAM translates a generated address to the actual geometrical address on the DUT. The topological RAM is loaded via TOPO X data, Y data where x and y data are positive values and less than 377 (octal). To use the topological scrambler (RAM), the simple instruction SCRM 1 enables and starts the process. Even though data patterns are generated as a function of address, they are independent of the initial address sequence, and thus, the user can scramble the x and y coordinates and leave the patterns intact.

Data generation instructions can be used to define and select data patterns in one of three ways:

- Select one of 15 different data equations without requiring software intervention.
- Use the data RAM for logic combinations of selected data equations.
- Use the shift data register in repeating mode or to generate pseudorandom data.

Data Equations. There are four sets (0 to 3) of hard-wired data equations in the pattern processor. The user can select a data equation (DE) or a data equation with its outcome inverted to its binary complement value

Table 5-5 PPM Compare and Chip Select/Refresh Instructions

Instructions	Mnemonic
Compare Equal (fld1) = (fld2)	CE fld1, fld2
Compare Greater than (fld1) > (fld2)	CG fld1, fld2
Disable/Enable Chip Select	CHPS 0/1
Disable/Enable Refresh	RFEN 0/1

(IDE). The basic equations selectable under program control are shown in table 5-6.

Each set corresponds to one of the four primary data channels to the memory-under-test (via the pipeline). If, for example, the user is testing a 256 x 4 memory, a different data pattern can be programmed into each of the four channels of the memory-under-test. Refer to figure 5-5 for generation and selection of data equations.

Logic combinations of Data Equations. The pattern processor data RAM extends the basic data generator by providing the capability to make any logic combination of the basic equation listed in the preceding table.

For example, the equation $X = X_2$ represents a single row bar at the programmed value of X_2 . The equation $X = X_3$ represents a single row bar at the programmed value of X_3 . Note that both X_2 and X_3 are changeable under program control at test speeds without breaks in testing. With the data RAM, the user can program the equation $(X = X_2) + (X = X_3)$ which is a double row bar.

Combinations of up to four logic equations can be accomplished with the data RAM; combinations like (equation 1) + (equation 2) (equation 3) + (equation 4).

The data RAM is implemented with four 16-word by 4-bit memories that are user-programmed to create the desired logic combinations. Programming is accomplished via a definition instruction: DATA (n1), (n2), (n3), (n4) where n1, n2, n3, and n4 are four-bit octal numbers that load into the respective 16 x 4-bit RAM memories.

To load the data RAM, an ORG statement positions the storage address register to the desired word in the RAM; DRAM enables access to the data RAM; and the RMUX instruction specifies which of the four-bit patterns is desired.

Use of the shift data register allows deviations from the hard-wired data equations. Data generation via the shift data register provides repeating or pseudo-random patterns.

LSHFT 1 enables the shift register. If, with the RNDM instruction, the user selects operation mode 0, the shifter generates data that repeats ever 16 cycles. This is done by the end-around shift of the contents of the 16-bit shift register with each bit being shifted one place from lowest to highest order bit.

If the user selects RNDM mode 1, the shifter generates pseudorandom data that repeats ever $2^{16} - 1$ cycles. Each bit is shifted one place as before. Then bit 0 is inverted and exclusive-ORed with bit 15. The resulting binary value is held as reserve to be shifted into the lowest-order bit for the next data pattern generation.

Fig. 5-5 Generation and Selection of Data Equations

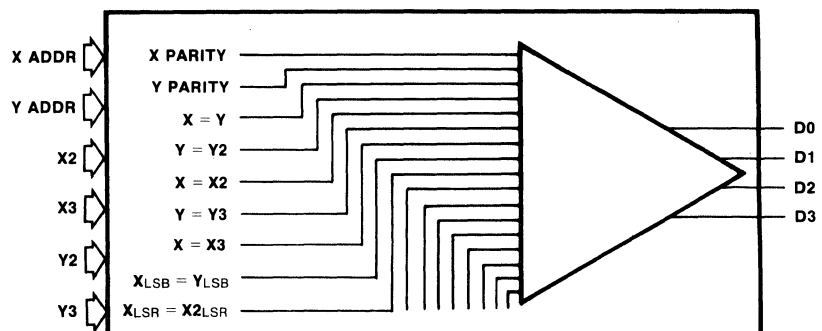


Table 5-6 Data Equations

Select-Number	DE0	DE1	DE2	DE3
0	(X Parity) XPAR	(Y Parity) YPAR	(Diagonal) X = Y	(Checkboard) X = YL
1	(Diagonal) X = Y	(Diagonal) X = Y	X = X2	(Row Bar) X = X2L
2	(Spiral) X = Y + X2	X = X2	Y = Y2	(Column Bar) Y = Y2L
3	X = X2	X = X3	SHIFT2	SHIFT3
4	X = X3	Y = Y2		
5	Y = Y2	Y = Y3		
6	Y = Y3	0		
7	(All Zeros) 0	SHIFT1		
8	(Y Parity) YPAR			
9	(Checkerboard) X = YL			
10	(Row Bars) X = X2L			
11	(Column Bars) Y = Y2L			
12	(Row Bars) X = X3L			
13	(Column Bars) Y = Y3L			
14	(One Pattern) (X = X2) (Y = Y2)			
15	(Random Pattern) SHIFT0			

Data Generation Instruction	Mnemonic
Normal Data Equations	DEn select-number
Invert Data Equations	IDEn select-number
Select subfield in Data RAM	RMUX integer (0 to 3)
Enable/Disable Data Shifter	LSHFT 1/0
Enable/Disable Random Mode	RNDM 1/0
Enable/Disable Data RAM	DRAM 1/0
Enable/Disable Topological Scrambler	SCRM 1/0
Reset Hardware FLAG and Invert Data	RST
No (Null) operation	NOP
Halt and branch to own address	HALT

Note: The X and Y are the working registers.

L means that the least significant bit of the working register is compared to the least significant bit of the specified register.

Branch instructions alter the execution sequence of the microprogram loaded into the control RAM. They can be part of either an address or a data generator word and give the user even greater flexibility in altering test sequences and patterns. Table 5-7 lists the branch instructions.

5.5 PPM Manual Analysis

Manual analysis of the memory under test is facilitated by five key commands: PAUSE, STOP, LOOP, READ, and WRITE.

STOP, in conjunction with PAUSE, stops testing within a specific microprogram at a particular location in the control RAM.

The LOOP command allows looping between address 0 of the control RAM and the address specified in the loop command.

READ allows the specified tester hardware register to be read and displayed immediately or at the next station pause. WRITE causes the tester hardware register specified to have the data written into it immediately or on the next station pause.

5.6 PPM Datalogging

The DATALOG command collects and reports memory failures in the memory-under-test. The command format is:

DATALOG FCT m COUNT STATxx

Where m is the additional number of failures (besides the very first one) to be datalogged, and where COUNT specifies that failures are datalogged by the test count of the tests that failed (rather than by datalogging failures by the local memory addresses at which the failures occurred), m can be as large as 8 million.

The printout for memory failures includes the statement number that initiated PPM operation, the test count of the test that failed, the X-coordinate value of the failure location in memory-under-test, the Y-coordinate value of the failure location, the failure data in binary, the expected data in binary, the function (type of test executed) that caused the failure (R or RW), and the value of the chip selected enabled.

5.7 PPM Diagnostic (PPOD)

The diagnostic package supplied with each pattern processor is composed of eight subprograms to verify the pattern processor. Execution of PPOD assumes that the system has passed all tests in TVFY, the Sentry system diagnostic package.

Table 5-7 PPM Branch Instructions

Instruction	Mnemonic	
Branch on True	BT	label
Branch on Not-True	BNT	label
Branch and save return	BSR	label
With BSR, the current Control RAM address plus one is saved in the Return Address register; then an unconditional branch is executed to the location specified in the instruction.		
Branch return	BRT	label
Branch unconditional	BRU	label
Branch on FLAG	BOF	label

The user can exercise PPOD three ways:

- Auto-execution of the entire verification with a printed system status.
- Individual-execution of each sub-program.
- Burn-in/repeated execution of the entire verification sequence at a requested repetition rate.

Console switch options give the diagnostic even greater flexibility, allowing halting on failures, cycling current tests, even walking through the sub-program step-by-step.

The functional PPOD sub-programs are:

- Register read/write test
- Control RAM memory test:
 - RAM counter increment test
 - RAM reset test
 - Read/write test
 - Walking 1 test (address Test)
- Address generator test:
 - Stop address test
 - Index data transfer test
 - Index delta transfer test
 - Index compare/branch test
 - Subroutine/flag branch test
- Data generator test:
 - Checkerboard walk test
 - Chip select and X/Y mask test
- Data out test
- Alternate TG4/period delay and width test
- Topological RAM memory test:
 - RAM Counter Increment Test
 - RAM Reset Test
 - Read/Write Test
 - Address Test
- Data RAM memory test:
 - RAM Counter Increment Test
 - RAM Reset Test
 - Read/Write Test
 - Address Test

Table 5-8 PPM Pin Assignments**TESTER PIN ASSIGNMENTS (FIXED)**

Tester Pin Function		Tester Pin Function	
1	XO	31	DI4 (=0)
2	X1	32	DO4 (=0)
3	X2	33	DI5 (=1)
4	X3	34	DO5 (=1)
5	X4	35	DI6 (=2)
6	X5	36	DO6 (=2)
7	X6	37	DI7 (=3)
8	X7	38	DO7 (=3)
9	Write (selects test rate and timing generator)	39	DI8 (=0)
10	Read	40	DO8 (=0)
11	DI0	41	DI9 (=1)
12	DO0	42	DO9 (=1)
13	DI1	43	Spare
14	DO1	44	Spare
15	CS1	45	DI10 (=2)
16	YO	46	DO10 (=2)
17	Y1	47	DI11 (=3)
18	Y2	48	DO11 (=3)
19	Y3	49	DI12 (=0)
20	Y4	50	DO12 (=0)
21	Y5	51	DI13 (=1)
22	Y6	52	DO13 (=1)
23	Y7	53	DI14 (=2)
24	CS2	54	DO14 (=2)
25	CS3	55	DI15 (=3)
26	CS4	56	DO15 (=3)
27	DI2	57	DI16 (=0)
28	DO2	58	DO16 (=0)
29	DI3	59	DI17 (=1)
30	DO3	60	DO17 (=1)

NOTE:

Pins 31-60 can be used as data pins for memories with up to 18 data lines by enabling Data Extension.

Dynamic Fail Module (DFM)

The Dynamic Fail Module (DFM) is an option designed for dynamic collection of fail data from memory and random devices. The DFM operates concurrently with the functional test equipment of the Sentry:

- Pattern Processor Module (PPM)
- Local Memory (LM)
- Local memory equipped with Sequence Processor Module (SPM)

Basically DFM performs two functions:

1. Continuous data collection of multiple functional failures while a device is being tested at high speed for large memory arrays by using either the SPM or LM/SPM.
2. Data collection and masking functions for both PPM and LM/SPM testing.

DFM software is implemented under Sentry's MASTR software operating system. This allows the user to control completely the DFM from a FACTOR device program or from DFM commands entered through any Sentry command device, including manually from a VKT.

6.1 Operating Modes

The DFM may be programmed to operate in one of ten modes. The modes are used when testing memories using the Pattern Processor Module (PPM) or when testing random logic devices with the Sentry Local Memory (LM) and/or Sequence Processor Module (SPM). Table 6-1 identifies the ten DFM modes and indicates the tester functions with which they are designed to operate.

6.1.1 Memory Wrap Around

The memory wraparound feature controls the filling of the location memory. Normally, when the DFM is in one of its data collection modes, location memory is filled with X, Y address data (PPM use) or test number data (LM use) from top to bottom (word 0 through 2047). When it is completely loaded, it stops collecting data.

If the memory wrap around feature is enabled the DFM overwrites the Location and Data Memories after they have been completely loaded. At End-of-Test, data from the last 2048 fails is available to be examined or printed with the various DFM reports.

The FAIL counter indicates the actual number of fails detected. The fail counter can also be used with the FAIL DETECT ENABLE feature to ignore a specified number of tests before starting to count fails. The maximum number of tests that can be ignored in this mode is 16,777,215. Any fail occurring after this point is detected and, depending on the mode, the appropriate data collection or masking functions are performed.

6.1.2 Fail Detect Enable Feature

The FAIL DETECT ENABLE feature allows a DUT to be initialized. While DUT initialization is in process, any functional fails that occur are ignored (not detected) by the DFM.

The user programs the START counter to the number of tests to ignore. The START counter is filled in two's complement format by the DFM software overlays. As tests are applied to the DUT, the START counter is incremented. All fails are ignored and no data collection takes place. When the START counter reaches zero, the fail detect mechanism is enabled. Any fail occurring after this point is detected and, depending on the mode, the appropriate data collection or masking functions are performed. These features may be enabled or disabled as appropriate with all DFM modes.

6.2 DFM Operations

The DFM may be programmed to perform three initializing operations: RESET, CLEAR MEMORY TO ZERO, and CLEAR MEMORY TO ONE. When programmed these operations are performed immediately.

6.2.1 Reset Operations

The RESET operation causes all the logic in the DFM control section to be reset.

The three counters, START, TEST and FAIL are all set to zero. The programmable bits in the DFMS register are not altered; thus any programmed mode functions will remain enabled.

The station RESET button resets everything and places the DFM in IDLE mode.

6.2.3 Clear Memory Operations

Two clear memory operations are available: CLEAR MEMORY TO ZERO sets the DFM memory to zeros; CLEAR MEMORY TO ONE sets the DFM memory to ones. Both the location memory and the data memory are affected.

6.3 DFM Report Formats

The DFM software package provides a selection of seven different report formats. The report types and their descriptions are summarized in Table 6-2.

The reports can be initiated by a FACTOR device program or by DFM commands and printed on the primary output device. For report formats involving large memories, the user may optionally select portions of the report to be printed. The cell failure and content reports may be printed by the sections indicated in Table 6-3.

Table 6-1 Modes, Features, Operations DFM Modes

Mode	Test Function	Description
*ACCUMULATE	PPM	Used when testing memory devices with the PPM. Expected, Fail, and X, Y address data is collected into the DFM.
*ACCUMULATE/MASK	PPM	Similar to Accumulate mode, except that the DFM collects Expected, Fail, and X, Y address data only on the first failure detected in each device memory. When a bad cell is tested several times all failures except the first are masked.
*MASK	PPM	Used to test memory devices and to ignore failures in previously selected cell locations.
*MASK AND HALT	PPM	Same as the Mask mode with one exception; when the first new unmasked failure is detected, testing is terminated. The location memory and expected data sections are not used.
*PASS/FAIL	PPM	Causes the DFM to continuously store Expected and Fail data into the data memory regardless of whether the test vectors pass or fail.
*COLLECT FAIL DATA	LM	Collects Fail data resulting from LM functional testing. If memory wrap around feature is enabled with the Collect Fail Data mode the DFM collects data in a circular fashion. In this case DFM will contain the data from the last 2048 failing test vectors.
*HALT ON TEST	PPM or LM	Causes the tester to HALT after a specified number of functional test vectors are applied to the DUT. The maximum number of tests is 16,777,215. Functional tests may be applied with either PPM or LM.
*HALT ON FAIL	PPM or LM	Causes the tester to halt after a specified number of functional failures have occurred. The maximum number of functional fails is 65,535.
*HALT ON TEST/FAIL	PPM or LM	This mode is a combination of the HALT ON TEST mode and the HALT ON FAIL mode. When either of the two halt conditions occur, the tester is stopped.
*IDLE	- - -	Causes the DFM to discontinue operation. The DFM should always be in the IDLE mode when not in use.

*Require 1-bit, 4-bit, 8-bit or 16-bit Configuration

6.4 Module Configuration for PPM Usage

The pattern processor module is designed to test memory devices. Under program control it generates 16 X, Y address bits and from 1 to 16 data bits. These bits are all applied to the DUT during each functional test. The X, Y address bits select the "cell" within the memory to be written or read. For writing, the data bits are written into the cell. For reading, the data bits become the "Expected Data". The actual bits read from the memory is expected data to determine if the cell passed or failed.

When testing with the PPM the user must specify one of four possible Data Memory configurations. The configuration should correspond to the number of data lines on the memory as shown in Table 6-4. Early RAMs which typically had one data line are tested with the DFM in the "1 Bit" configuration; memories with 2, 3, or 4 data lines are tested with the DFM in the "4 bit" configuration, etc.

Whether the user is testing memory with 1, 4, 8, or 16 bits word. Table 6-5 shows the memory device sizes that may be supported by the DFM.

Figure 6-1 is a block diagram of the DFM as viewed for PPM use. The data memory is divided into two sections: one section is used to collect fail data, the other is for expected data. The two sections are each mapped into 1, 4, 8 or 16 bit wide "cells". Thus, for each cell of the DUT there are two corresponding cells in the DFM. These cells are addressed by the PPM's X, Y addresses. The fail data and expected data are stored into the memory in accordance with PPM addressing algorithms.

Table 6-2 DFM Report Summary

Report Type	Description
Cell Failure Report	Used to view a memory device in terms of its good and bad cells.
Cell Content Report (Binary)	Displays (in Binary format) the contents of a memory device after testing in PASS/FAIL mode.
XY Address Report	Displays the contents of Location Memory after memory testing in PASS/FAIL or ACCUMULATE modes.
LM Fail Data Report	Displays the contents of the DFM memory modules after testing, via Local Memory, in COLLECT FAIL DATA mode.
Module Content Report	Displays the contents of the DFM memory modules.
Status Report	Displays the contents of the DFM Mode and Status register and the START and FAIL counters.

Table 6-3 Data Memory Configurations for PPM Use

Max. RAM Size	Configuration	Section Number	X (Row) Coordinate	Y (Column) Coordinate
64k	1-bit	1	0-63	0-63
		2	0-63	64-127
		3	0-63	128-191
		4	0-63	192-255
		5	64-127	0-63
		6	64-127	64-127
		7	64-127	128-191
		8	64-127	192-255
		9	128-191	0-63
		10	128-191	64-127
		11	128-191	128-191
		12	128-191	192-255
		13	192-255	0-63
		14	192-255	64-127
		15	192-255	128-191
		16	192-255	192-255
16k	4-bit	1	0-63	0-63
		2	0-63	64-127
		3	64-127	0-63
		4	64-127	64-127
8k	8-bit	1	0-63	0-63
		2	0-63	64-127
4k	16-bit	1	0-63	0-63

Table 6-4 RAM Sizes Supported by DFM

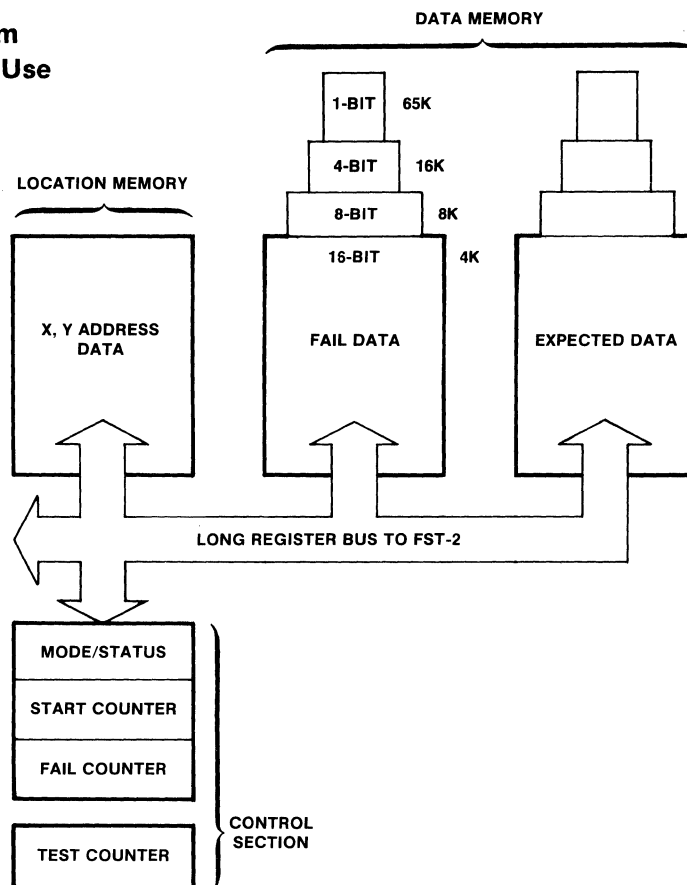
RAM SIZE (CELLS)	MAX ROWS (X)	MAX COLUMNS (Y)	MAX DATA LINES (Z)
65536	8	8	1
16384	7	7	4
8192	6	7	8
4096	6	6	16

The location memory is filled with the X, Y address words of the memory cells that fail. The format of each word depends upon the specified configuration. Location memory is filled from top to bottom (words 0 through 2047) as failures are detected.

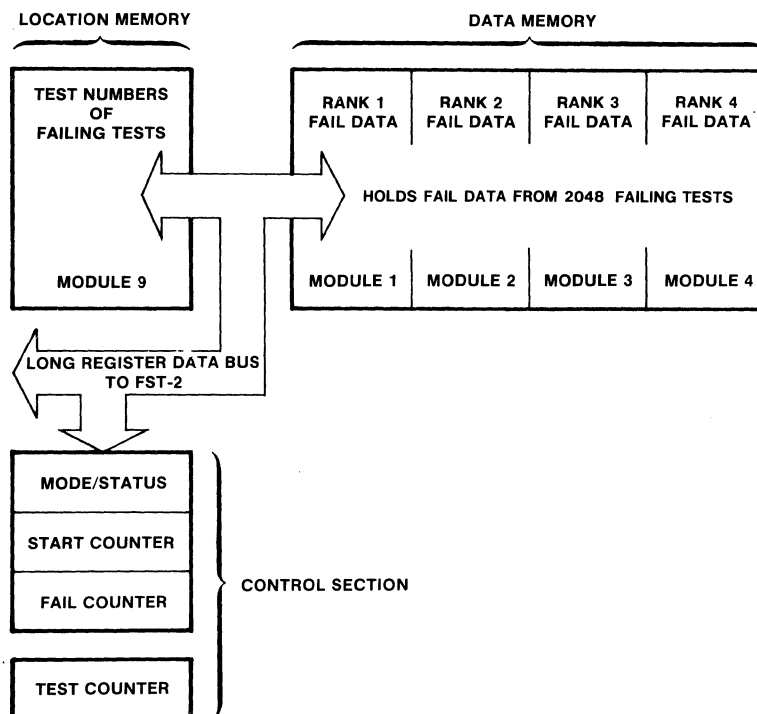
6.5 Module Configuration for LM Usage

Figure 6-2 is a block diagram of the DFM as viewed for LM use. When testing with the local memory or sequence processor module, the COLLECT FAIL DATA mode is used to collect fail data. The fail data are stored into data memory as each functional fail occurs. Fail counts are stored into the Location Memory.

**Fig. 6-1 Functional Block Diagram
of DFM Viewed for PPM Use**



**Fig. 6-2 Functional Block Diagram
of DFM Viewed for
LM Use**



Control Section

The DFM control section provides DFM addressing and timing functions. It also contains the START, FAIL and TEST counters and the mode and status register. The mode and status register determines which of the various DFM features, operations and modes are enabled. The counters are described in the following paragraphs.

The 24 bit START counter is used to ignore a specified number of test vectors or to halt the tester on a specified test vector. During normal data collection or masking operations the START counter is used to count the test vectors. At end-of-test it contains the test number of the first failing test vector; this count excludes the number of tests that were ignored. The maximum test vector count "T" is 16,777,215.

The 16 bit FAIL counter counts the number of fails detected by the DFM during a particular test sequence. The counter is enabled when the FAIL DETECT ENABLE condition exits. Its contents indicates the number of fails collected into the DFM memories. The maximum fail count is 65,535.

The 20 bit TEST counter counts the number of tests applied to the DUT after a failure has been detected. Its contents are stored in the local memory in COLLECT FAIL DATA mode for LM testing. This counter provides a maximum test count of 1,024,000.

DFM Report Examples

6.7.1 Cell Failure Report

DFM CELL FAILURE REPORT
SECTION: 4

DUT SIZE: 128 BY 128 DATA: 4
(X-DOWN Y-ACROSS *-BAD CELL)

[illegible]

Cell Content Report (Binary)

```
DFM CELL CONTENT REPORT      DUT SIZE: 128 BY 128  DATA: 1
SECTION: L  DATA LINE: 1    (X-DOWN Y-ACROSS)  BINARY
```

111111111122222222223333333333444444444455555555556666
012345678901234567890123456789012345678901234567890123

[illegible]

Cell Content Report (HEX)

```
DFM MASK MEMORY REPORT      DUT SIZE:  64 BY 64  DATA:  8
SECTION:  1  DATA LINE:  5- 8  (X-DOWN Y-ACROSS)
```

111111111122222222223333333333444444444455555555556666
012345678901234567890123456789012345678901234567890123

```

0 FFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFF
1 FFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFF
2 FFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFF
3 FFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFF
4 FFFFFFFF00000000FFFFFFFF00000000FFFFFFFF00000000FFFFFFFF00000000
5 FFFFFFFF00000000FFFFFFFF00000000FFFFFFFF00000000FFFFFFFF00000000
6 FFFFFFFF00000000FFFFFFFF00000000FFFFFFFF00000000FFFFFFFF00000000
7 FFFFFFFF00000000FFFFFFFF00000000FFFFFFFF00000000FFFFFFFF00000000
8 FFFFFFFF00000000FFFFFFFF00000000FFFFFFFF00000000FFFFFFFF00000000
9 FFFFFFFF00000000FFFFFFFF00000000FFFFFFFF00000000FFFFFFFF00000000
10 FFFFFFFF00000000FFFFFFFF00000000FFFFFFFF00000000FFFFFFFF00000000
11 FFFFFFFF00000000FFFFFFFF00000000FFFFFFFF00000000FFFFFFFF00000000
.
.
.
```

6.7.4 XY Address Report

DFM	XY	ADDRESS	REPORT	DUT	SIZE:	128 BY 128	DATA:	4
FAIL	"X"	"Y"	EXPECTED DATA	FAIL DATA				
1	0	0	1111	1110				
2	0	9	1111	0010				
3	17	255	1111	0010				
4	0	0	1111	1110				
5	17	255	0000	0010				

6.7.5 LM Fail Data Report

TEST NO.	PIN NO:	1	1	2	2	3	3	4	4	5	5	6
	5	0	5	0	5	0	5	0	5	0	5	0
229	000011110000111	111111111111111	000000000000000	000000000000000								
344	000000000000010	000000000000000	000000010000000	000000000000000								
345	000000000000010	000000000000000	000000010000000	000000000000000								
975	000011110000111	111111111111111	000000000000100	000000000000000								
1543	000000000000010	000000000000000	000000000000000	000000000000000								
1544	000000000000010	000000000000000	000000010000000	000000000000000								
26422	000000000000000	000000000000000	000111110000000	000000000000000								
26478	000000000000010	000000000000000	000111110000000	000000000000000								
26502	000010000000000	000000000000000	000000000000000	000000000000000								

6.7.6 Status Report

	DFM STATUS REPORT
PPM	PASS/FAIL
(51470)	4 BIT MODE
	START: 155 WRAPAROUND
	FAIL: 2047

	DFM STATUS REPORT
LM	COLLECT FAIL DATA MODE
(27430)	START: 0
	FAIL: 35

6.7.7 Module Content Report

ADDRESS	CONTENTS OF MODULE 3 (OCTAL)	
OCT	DEC	
0120B	0080.	177777 177777 177777 177777 177777 177777 177777 177777
0130B	0088.	177777 177777 177777 177777 077777 177777 177777 177777
0140B	0096.	177777 177777 177777 177777 177777 177777 177777 177777
0150B	0104.	177777 177777 177777 177777 177777 177777 177777 177777
0160B	0112.	177777 177777 177777 177777 177777 177777 177777 177777
0170B	0120.	177777 177777 177777 177777 177777 177777 177777 177777
0200B	0128.	177777 177777 000000 177777 177777 177777 177777 177777
0210B	0136.	177777 177777 177777 177777 177777 177777 177777 177777
0220B	0144.	177777 177777 177777 177777 177777 177757 177777 177777

System Software

7.1 General

Using the Sentry system software, it is possible to load the system, perform various tests on a device, and obtain go/no-go results, and perform diagnostic tests. Test results may be printed out, recorded on the disc memory, CPU memory, magnetic tape, or on the Integrator, or displayed on the video keyboard terminal, or a combination of the above devices, depending on the peripheral equipment selected for use.

System software is supplied as object and data material on 9-track 800 bpi magnetic tape with the CPU and peripheral diagnostics in source and object code on the magnetic tape.

Standard system software is delivered as an integral part of each hardware system at no additional cost, and undergoes a complete verification by the FTSG field engineering staff upon system installation.

7.2 MASTR System Software

MASTR (Managing A Sentry Tester) is a multi-task real time operating system designed to control the functions associated with testing, generating test programs, and characterizing complex digital integrated circuits.

System software consists of the resident programs of the operating system and overlays. The monitor and the test head driver programs are resident once the system is booted into memory. An overlay is an assembly language program and is loaded into memory to perform a particular function, and then can be released from the memory when the function is completed. The system organization is illustrated in figure 7-1.

7.2.1 Peripherals Supported

The software supports various peripheral configurations. A simplified block diagram showing the information flow of the Sentry VIII system is shown in figure 7-2, the information flow through the peripherals is also illustrated. The system requires at least one program storage device (a disc, a magnetic tape unit, or an Integrator) but programs may be stored on any of these media if the system is equipped with more than one storage media.

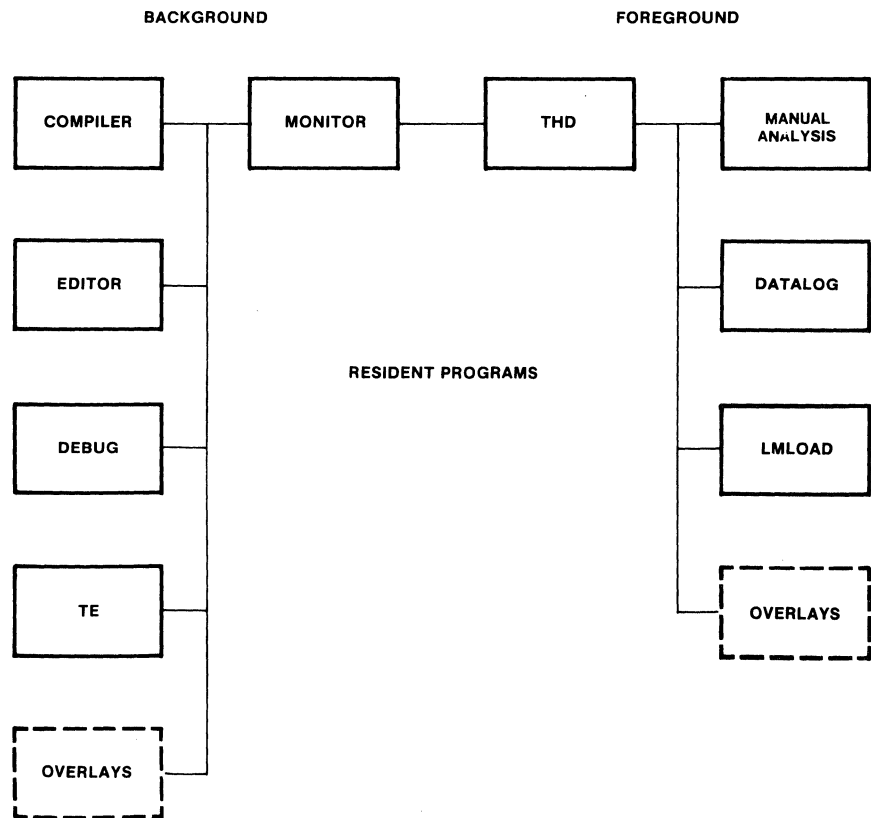
7.2.2 External Interfaces

The general purpose instrument port is compatible with the IEEE/488

- 1975 Standard Digital Interface for programmable instruments. This allows the Sentry software a convenient means for programming up to 14 instruments.

The communications link is RS232C compatible with baud rates up to 9600. The Sentry system software is designed to use a message and line protocol (Bell 202S compatible) including error detection, that links the Sentry to the Integrator host processor. The link may be either hard-wired or connected from telecommunications equipment. Incorporation of this communications link allows the Sentry to datalog to the Integrator as well as utilize the mass storage of the Integrator for up-loading and down-loading of test plans, source files, and ALLINK files. For specific information related to the Integrator, refer to the Integrator Product Description.

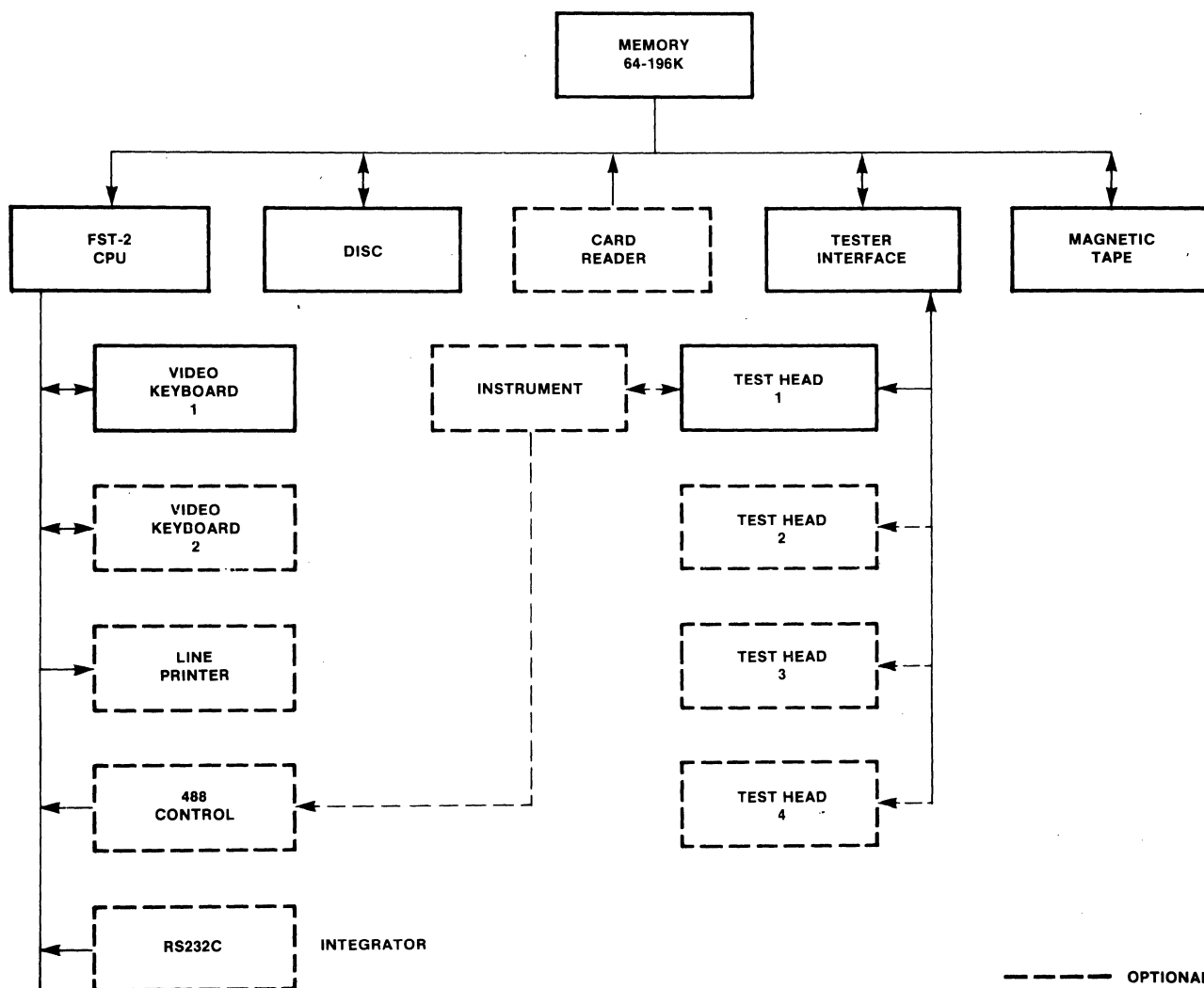
Fig. 7-1 Software Architecture



7.2.3 MASTR Monitor

The MASTR monitor program monitors the operator requests, schedules required activities, initiates execution of scheduled programs, manages memory usage, controls I/O peripheral usages, and controls program activity and traffic between foreground and background programs.

Fig. 7-2 System Information Flow

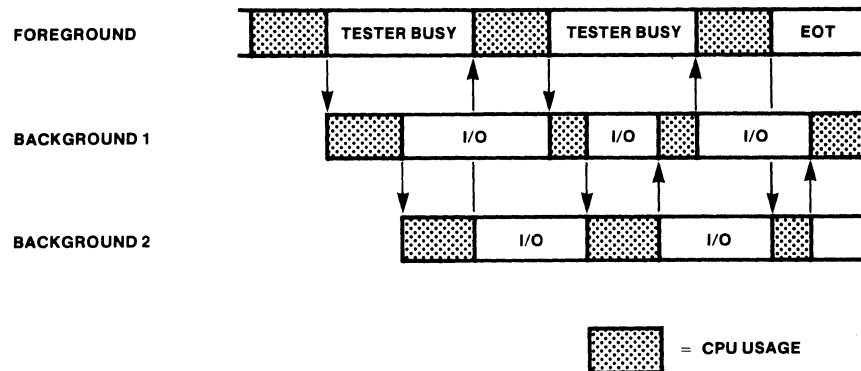


7.2.4 Foreground/Background Tasks

Any function that is directly related with testing and the tester hardware is considered a foreground task. Foreground tasks can be used for executing a test program, collecting data from the local memory or reading of tester registers. All other functions which are not directly related with testing are considered background tasks. Background tasks can be used for compiling a test program, loading an overlay into memory or editing a program. A tester operation requested by an operator command is performed in the background. The foreground may be locked out during these special cases.

Foreground tasks have a higher priority than do background tasks and the monitor provides as much time for foreground tasks as possible. Execution control is returned to the background task whenever the tester hardware becomes busy, allowing the CPU to be used for other tasks. Background tasks normally give up execution control to foreground tasks or other background tasks while the peripherals are busy due to I/O operations. Examples of foreground/background switching are illustrated in figure 7-3.

Fig. 7-3 Foreground/Background Switching Under the MASTR Operating System



7.2.5 Test Head Driver

The Test Head Driver (THD) is a resident program that runs in the foreground and performs activities of the test stations, like:

- Responding to start requests
- Test plan execution in DMA or interpretive mode
- Displaying pass/fail information
- Calling foreground overlays

The THD is divided into three sections:

- Test controller
- Interpreter
- Arithmetic processor

The test controller initiates testing, prepares datalogging or analysis information, keeps track of pass/fail conditions, and starts DMA sequences. The interpreter prepares tester register data by scaling values and sets and resets tester registers. The arithmetic processor manipulates arithmetic expressions, manages the run-time-stack, performs control functions such as calling a subroutine or conditional branching and handles FACTOR I/O statements.

7.3 System Overlays

System overlays consist of foreground, background, and foreground/background overlays. These overlays may be loaded or released at any time based on the requirements of the particular operation. Some overlays may be used in foreground or background. Overlays loaded from the test program using the EXEC statement are executed as a background task. Table 7-1 contains an alphabetical list of some of the system overlays that are available.

7.3.1 Dual VKT Usage

The MASTR software provides the capability to support two VKTs. At least one VKT is required. The second VKT is optional on both the Sentry V and the Sentry VII.

7.3.2 Data Management Routines

The MASTR software provides the capability for fully debugged data management operations. A full range of arithmetic computation routines can be accomplished with the Sentry. The FST-2 computer can manipulate that data to produce histograms (including maximum, minimum, mean, standard deviation), floating point calculations, wafer mapping, Boolean expressions, etc. This provides instant data analysis capability so that changes can readily be assimilated by the test or evaluation engineer for immediate response or action while normal testing continues.

Additional datalogging features include datalog for collecting multiple fail responses on dynamic devices; selection of the desired data on a pass/fail per test, per device or per nth device basis; datalog to any I/O device including VKT, line printer, magnetic tape, or Integrator. The Sentry FACTOR programming language permits, by its structure, enhancements or the addition of special features to the already extensive datalog capabilities.

7.4 Test Programming Language

Programming of the Sentry is in an English-like language similar to FORTRAN or ALGOL-60. The Sentry language is called FACTOR (Fairchild Algorithmic Compiler Tester-ORiented). FACTOR provides two basic types of statements:

1. Arithmetic and logical control statements, such as those which normally comprise procedural languages.
2. Test control statements that set up and execute functional/parameter tests.

The Sentry compiler assists the programmer in the development of FACTOR test programs by indicating syntax errors committed, the statement length, etc. Thus, programming time is minimized because the effort is focused on the actual test rather than on grammatical errors.

Assembly language programs can also be used with the Sentry to minimize test program memory usage and overhead time; users of the Sentry can be trained in assembly language programming and can either write their own programs or work with Fairchild in program development.

7.5 Supplemental Software

7.5.1 Device Test Program Software

FTSG applications engineers generate programs and applications notes to assist in the programming of especially difficult or tricky devices. Field applications engineers are available also to assist new customers

in system use, generation of test programs, application routines, explaining of new or special system features, and to generally assist with troublesome device testing. Device test programs available cover virtually every class of semiconductor in all current functional product types: bipolar MSI/SSI, MOS static or dynamic MSI/LSI/VLSI (PMOS, NMOS, CMOS), memories (RAMs, ROMs, PROMS), calculator chips, watch circuits, low power devices, microprocessors, opto electronic devices, linear components, and micro-logic.

These test programs are placed in peripheral storage by the operator using the appropriate media and may be called into the system's central processor to enable the test system to apply specific parametric and functional testing parameters to the particular device under test. Test program media depends on the system peripherals specified in the particular configuration. The standard medium is 9-track 800 pbi source magnetic tape. However, test program packages are delivered to the particular medium - punched card, paper tape, magnetic tape, microfiche, etc. - appropriate to the user's specific hardware.

Applications support is available to every FTSG test system user and supplements the standard test programs and utilities. New devices, more pins, changed circuits, technical requirements evolving constantly, new management data, reformatted process control data - all these special situations may call for new, special-purpose software beyond the standard, available modules and packages. Custom software from Fairchild is available on special request, estimated to your testing needs.

7.6 Software Diagnostics

Extensive diagnostic software is provided as standard with all Sentry systems. The diagnostic software is designed to assist the customer in calibration, verification, and maintenance of the Sentry. With it, the performance of the entire system is measured or exercised for value, timing or function.

The diagnostics perform both macro and micro functions by defining a general malfunction area for one part of the system, peripherals or the interface, while pinpointing relay or other key component problems on the pin electronic cards. All elements of the test system, the CPU, memory, long and short registers, timing generators, drivers, comparators, certain relays, the Precision Measurement Unit (PMU), the peripherals, and the peripheral interface are systematically examined by the diagnostics. The PMU is used, after its self-check with standard resistors, to measure the various parts of the system for DC accuracy, not just functional verification.

At the request of the operator, selected portions of the diagnostics can be exercised; they can verify the operation characteristics, accuracy, tolerances, and limits of the tester hardware itself to establish confidence in the performance and condition of hardware elements as well as assure the functional operation of the system architecture. The diagnostic package provides programs to completely check out the mainframe, the computer, the test station, and all system peripherals.

A powerful set of diagnostic software, taking from two to thirty minutes to run, has direct impact on profit and loss for every customer since failure modes are readily identified and rapidly corrected; thus, wasted personnel and dollar losses due to production slow downs are minimized, with a resulting favorable impact on dollar savings.

Table 7-1 MASTR Overlays

Overlay Name	Description	Called From
COPY	Copy overlay is used to copy any type of file from any peripheral or memory to any other peripheral or memory.	Background
CYCLE	Used as a debugging aid to allow the user during the execution of a device test program, to establish a continuous loop between two specified addresses in local memory. Any optional sync pin number and vector location may also be provided.	Foreground/ Background
DIST	Used to collect parametric test results and sort them into distribution curves.	Foreground/ Background
DL	Used to log test results such as fail logging, DC fail or measurement logging, pattern processor memory fail logging, and EOT logging.	Foreground/ Background
DLREG	Allows displaying of long pin registers at specified cycle count of local memory execution.	Background
EDIT	Allows editing or generation of source programs via operator entered directives.	Background
FST	Functional sequence trace overlay allows display or listing of the sequence of pin data for any specified region of a functional test pattern.	Foreground/ Background
GETXY	Used with SPM and PPM to return functional fail information.	Foreground
GLOBS	An optional overlay which allows the user to specify additional global variables for each station.	Foreground
IBUS	Allows communication from a FACTOR program with instruments via IEEE-488 standard bus.	Foreground/ Background
LABEL	Allows generation of messages in large block character type format.	Foreground/ Background
LMIO	Local memory I/O overlay is used to speed test program development and debugging by allowing functional test data	Foreground/ Background

	to be transferred between local memory and output devices. Execution is accomplished in an interaction mode via the VKT and allows repetitive access to any section of local memory.	
LMLOAD	Local memory load overlay allows transferring of functional test data between local memory and files on disc or memory at run time.	Foreground
LMSAVE	Local memory save performs the same functions as LMLoad, however, in addition it is used in conjunction with microprocessors and test generation programs. Converts hexadecimal or octal and also converts microprocessor opcodes to their mnemonics for output.	Foreground
LPLF	Line printer line feed allows positioning of the line printer paper from a FACTOR program.	Foreground
MBUP	Memory backup overlay is used to write the contents of main memory to mag tape.	Background
PPLOG	Pattern Processor data-logging overlay is a specialized datalogger which produces a failmatrix map of the RAM test pattern being executed by the Pattern Processor.	Foreground/ Background
PSCAN	Pin scan overlay is used as a diagnostic and analysis aid of FACTOR programs by scanning all programmed tester pins to establish a pin by pin program status of the test system. The status may be displayed on the VKT or printed on the line printer.	Foreground/ Background
PXLOG	Pattern execution log overlay allows observation of sequential events execution from PPM program execution.	Foreground/ Background
SPLOT	Automatically outputs an X-Y axis plot on the VKT or line printer via a FACTOR command or a Manual Analysis command. the plots can consists of timing and/or voltage deltas vs. DCT or functional pass/fails.	Foreground

TDX	Tape data transfer overlay is used as a file management tool for transferring groups of files between the disc or memory and tape.	Background
TE	Terminal error overlay displays a description of each terminal error.	Background
TTIME	Used to perform a binary search with a timing generator for the purpose of making time measurements.	Background
user overlays	Allows execution of user written assembly language programs as background overlays.	Background
VERIFY	Verify overlay generates an 8-digit number from any file type and displays the number or verifies that the file matches a verify number provided.	Background
VPLOT	An option allowing usage of Hazeltine 2000 VKT special features and point and vector plotting within a user defined window.	Foreground
WAIT	Allows execution of FACTOR test programs via MASTR memory or disc input files (MIF/DIF)	Background
XGRAPH	Used for graphic plotting of test results and other data. Among the plotting capabilities of XGRAPH are: schmoos plots, X-Y plots, and Bar graphs.	Foreground
XMIT	Transmit overlay allows dumping of the screen contents to the line printer. This permits convenient hard copy documentations of messages and other dialog between the operator and the system.	Foreground/ Background

Support Capabilities

Fairchild is committed to a complete systems approach for all products. Each Sentry system sold is complemented with complete hardware and software user oriented documentation and system training courses that are scheduled year round. You, as our customer, have access to a software and applications staff to solve your system needs, as well as a well-trained field service organization with spare-stocking offices worldwide.

Briefly, the Sentry is the most extensive and capable hardware and software test system on the market today. And the total support in service, training, applications and publications collectively is unmatched in the industry.

8.1 Customer Support

The Fairchild Customer Support Organization provides after sale support to FTSG customers through a worldwide field engineering group and a training group located at the San Jose headquarters facility.

Customer Support at Fairchild encompasses an inplant technical support group, a spare parts ordering group, a repair/exchange group, maintenance and programming training, a European service organization, and four-divisional United States service groups.

Fairchild maintains a world-wide field service engineering group for system maintenance and testing support to the customer. Factory-trained resident field engineers are strategically located throughout the world to provide on-site maintenance support.

Complete on-site service is provided for 90 days after completion of the system installation at the customer's facility under the standard system warranty. Service after the 90 day free service period may be contracted for as a maintenance agreement.

8.2 Service Maintenance Contracts

As a customer of Fairchild there exists a wide choice of service contracts. In summary the contracts available are:

- Fixed Price Maintenance - Under a fixed price maintenance agreement, a flat monthly fee is paid based on the size and complexity of the system, and, for this fee the customer receives automatic system software revisions, monthly calibration service, scheduled preventive maintenance, automatic incorporation of Field Change Notices, plus free parts and labor. An FTSG maintenance agree-

ment affords you the assurance that your products will be continuously maintained in top operating condition at a known and budgeted cost. The standard fixed price maintenance agreement covers on-call service eight hours per day, five days per week excluding holidays.

- Standby Plan - This plan guarantees availability of FST service personnel within four hours.
- Extended Coverage Plan - Multiple shift coverage (16 or 24 hour/day, five to seven days/week). Response time for extended coverage plans is within four hours of a request for remedial maintenance.
- Resident Field Service Engineer Plan - This plan is valuable if there are several large systems performing critical operations. This plan provides one resident field service engineer for on-site coverage one shift, five days per week (excluding holidays). Working hours may be adjusted to fit individual requirements. The cost of a resident field service engineer is a fixed price per month, plus parts and portal to portal relocation (where applicable).
- Extended Travel Option - Normal travel factored into the basic monthly maintenance prices covers travel within 100 miles of the FTSG service office. If the system is located more than 100 miles from the FTSG service office, FTSG offers an Extended Travel Option where a fixed monthly charge covers travel time to your location.
- Response Improvement On-Call Service - This plan guarantees response time will be within 24 hours. This type of on-call service is a flat rate per occurrence plus parts, materials, labor, travel expenses (including lodging and meals).

These types of service allow you to pick the most suitable arrangement for your testing system or systems and for operations at your facility.

Customers who prefer to employ Fairchild service on a time-and-materials basis may request service, parts and labor as they need them. This arrangement provides maintenance service as required at an hourly rate. Travel time is also charged at the applicable hourly rate. All parts and material are charged at established catalog prices. The customer is also charged miscellaneous expense of lodging, meals, car rental, mileage, and transportation charges such as airfare. This on-call service is, however, recommended for customers who have their own maintenance capability or whose sense of urgency, in terms of response time for service, is not critical. (While it is Fairchild's policy to respond as quickly as possible to all requests, service contract commitments receive priority.)

8.3 Spare Parts

FTSG offers to its customers spare parts kits to speed system repair. FTSG also offers a PC board repair/exchange program to relieve the customer of a critical situation as soon as possible on current production boards.

8.4 Training

Included in the purchase price of each Sentry system are 18 training credits (add one credit each for SPM and PPM options). Each credit equals one week of training in San Jose at the FTSG training center. Training classes range in length from one to three weeks. The training includes all manuals, schematics, and systems hands on training. It is recommended that training courses be attended during the months preceding the delivery of the system, so that each user will be ready to fully utilize the Sentry tester as soon as it is installed.

Training is conducted by FTSG instructors who are well versed in the latest device testing, computer technologies, programming, and education techniques. The training courses are scheduled over six month periods and courses may be added and deleted from the schedule according to customer requirements.

Three forms of training are offered, they are:

- On-site training at the customer's facility - This form of training is cost effective when the customer has groups of students who must travel a long distance for training, or when personnel to be trained are needed on a daily basis in their own facility.
- Training at the FTSG training center - This form of training provides the student modern teaching facilities to help the student learn in a controlled atmosphere with a training lab with the latest equipment as well as an in-house TV studio for viewing video tapes.
- Video Tape and audiocassette workbooks - This form of training provides an arm chair approach to learning and provides an excellent means for reviewing or bringing new personnel up to speed on the Sentry equipment. Video equipment may be rented from Fairchild.

A training catalog listing classes, costs and course descriptions is available on request.

A dedicated technical publications group comprised of professional technical writers and a complete production staff supports the Sentry product line. The publications department provides complete and comprehensive user-oriented manuals to support all phases of operation from programming to maintenance. A catalog of available publications is available on request.

Installation Requirements

9.1 Environmental Requirements

Even though the Sentry test system can operate in a temperature range of 15°C to +30°C (+60°F to 86°F) with a relative humidity level of 5 to 50%, non-condensing, Fairchild recommends an optimum temperature of 23°C (73°F) and a relative humidity level of 35%. This optimum environment provides the largest buffer in terms of system operation, accuracy, and guard band repeatability.

Deviations from the recommended environment, in either direction, for sustained periods will expose the system to possible malfunction. Deviations of 24 hours or more will permit cards, magnetic tape, paper, and electronic components to reach steady-state conditions and, thus, prolong return to the optimum design point.

High relative humidity levels may cause condensation, improper feeding of cards and paper, leakage which interferes with low current measurements, plus operator discomfort. Low humidity levels tend to increase the possibility of static charges which may cause intermittent interference with precision measurements.

Since moisture and foreign particle contamination tends to degrade precision high speed test equipment performance overtime, it is recommended that routine maintenance be performed to provide maximum instrumentation margins and sustained high levels of system performance.

It also recommended that automatic air conditioning be provided at the site for maximum system availability.

9.1.1 Sentry Air Conditioning Requirements

To allow for heat produced by personnel, instruments, and the Sentry use six tons of air conditioning to cool the installation site; use more if there is other machinery or equipment in the area.

The following is a calculation for partial air conditioning requirements: Since a Sentry with two test heads draws approximately 115 amperes total current,

$$\text{Power} = (115 \text{ A}) (115 \text{ VAC}) = 13.225 \times 10^3 \text{ VA}$$

The heating, ventilation, and air conditioning required is approximately 0.4 tons per kilowatt. $(13.225)(0.4) = 5.29$ tons TYP. Maximum of 6.2 tons.

9.2 Power Requirements

Sentry systems require a 3 phase, 5 wire drop with a rating of 50 amps per phase, voltage of 115/208V (Y-connected) and a frequency of 60 Hz (50 Hz optional).

The power to the peripherals (disc, card reader, line printer and video keyboard terminals, is to be supplied from separate 115 volt one phase outlets. These power lines do not come from the mainframe and should be removed from high emissive sources. Although separated from the primary system power, the source of peripheral ground should be physically no greater than 5 feet from the source of the systems primary power ground.

The power input must maintain voltage and frequency to within $\pm 5\%$. The variations can be tolerated without damage to the system, however, operating performance may be affected.

9.3 Space Requirements

Figure 9-1 shows a floor plan for the Sentry with one test station.

9.3.1 Sentry Mainframe

The central, control console consists of a single bay with side panels on each 44-inch (110 cm) side that are removable for servicing or maintenance or the internal electronics. The height of the SVIII mainframe is 70 inches (178 cm).

The magnetic tape unit, housed in the central console, is accessed by a hinged door that has a swing-out radius of 30 inches (75 cm.) The swing door on the opposite side of the central console covers the computer, memory, and I/O and has a swing-out radius of 20 inches (50 cm).

Three feet (90 cm) of access space should be left around the entire machine for maintenance.

9.3.2 Test Station

The test station is a single bay 35"x35"x35" (67.5 cm x 67.5 cm x 67.5 cm).

Within the test station is the pin electronics carousel designed to function as a manual station or with a wafer prober or automatic or environmental handler station. It can contain up to 30 pin electronic cards (60 pins) placed radially in a package configuration 16" (40cm) wide by 15" (37.5 cm) deep by 9" (22.5 cm) high.

The display and control panel is mounted in a portable box that can be placed at any location on the table top of the test station to suit the operator's convenience. The box is 9" (22.5 cm) wide by 7" (17.5 cm) deep by 3" (7.5 cm) high.

9.3.3 Peripherals

The VKT and card reader, require tables so that they are at a convenient height for use by the operator. A table area beside the VKT is useful for writing and for holding listings, information to be entered, run sheets, etc. Sentry customers may supply their own tables or order accessory tables from Fairchild

The fixed-head disc available with the Sentry is a free-standing unit 23" (58 cm) wide by 24" (61 cm) deep. Three feet should be left at the front and the sides of the disc console to allow for easy operator use of the disc and to accomodate maintenance personnel.

9.4 Flooring and Cabling

Although not absolutely necessary, the user may implement a 6"-8" (15-20 cm) raised floor for the installation site. With a raised floor, peripheral and power cables external to the mainframe are run under the floor to eliminate hazardous clutter. With or without a raised floor, test station cables are run through the cable duct included with each system.

9.4.1 Cable Length from Mainframe to Test Head

Although the physical length of the shortest cable that connects the high speed controller is 10 feet the actual usable length is 5 feet, due to cable routing in the test station. The high speed test station cable lengths are identical to the high voltage test head.

For those systems equipped with IEEE/488 instrumentation interface, a 2 meter limitation is made by the length of the interface cable from the controller to the performance board. This means that at least one station be located as per the suggested floor plan in Figure 9-1.

9.5 Equipment Weight

The approximate weight for the main items of the Sentry are as follows:

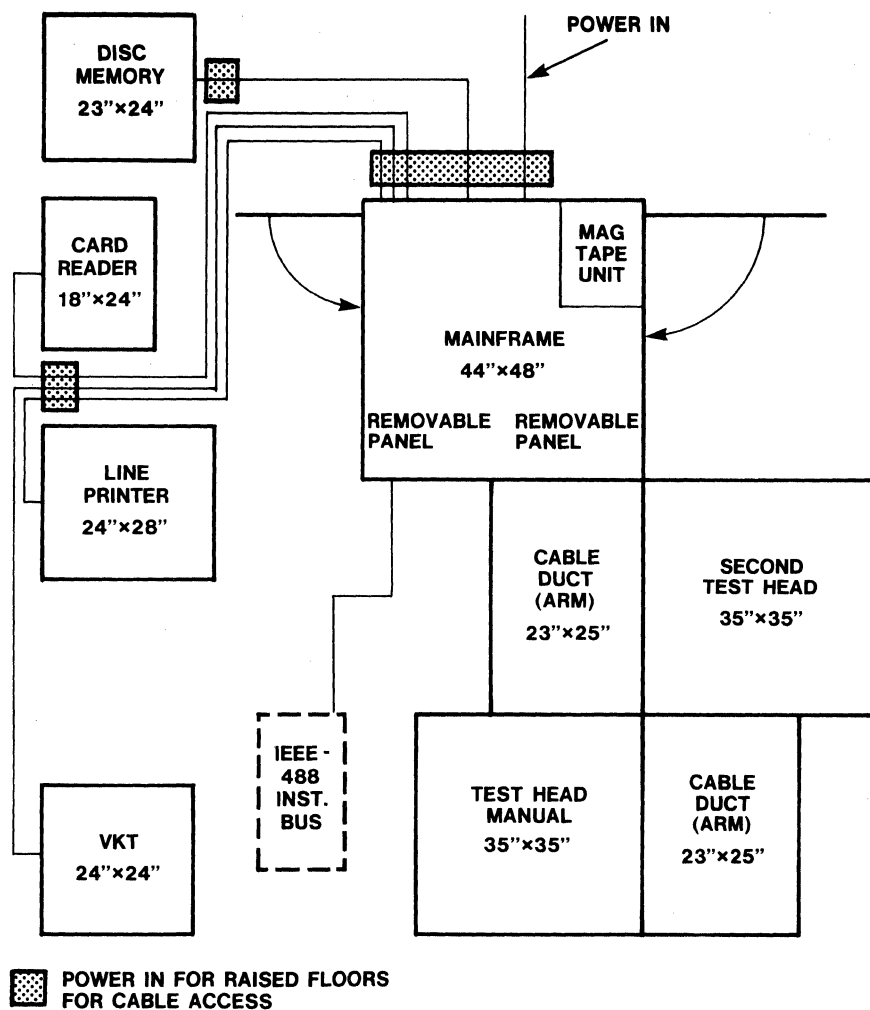
Mainframe: 2,000 pounds (907 Kg)
Test Station: 300 pounds (136 Kg)
30 pounds for the pin electronics
carousel and 4 pounds for the display
and control panel
Cable Duct Assembly: 100 pounds (45 Kg)
Disc: 450 pounds (204 Kg)
Card Reader: 45 pounds (20 Kg)
VKT: 40 pounds (18 Kg)
Line Printer: 230 pounds (104 Kg)

9.6 Accent Panel Colors

The Sentry accent panels can be ordered in one of four colors to suit your facility's color scheme.

Deep Wafer Blue (Federal Standard #15180)
Ranch Red (Federal Standard #31136) Standard system color
California Gold (Federal standard #33434)
Sunset Orange (Federal standard #31136)

Fig. 9-1 Typical Layout



Recommended Measurement Equipment and Spare Parts

Fairchild recommends that the Sentry system user gather the following list of instruments for use at system installation time and for subsequent device program debugging.

- Hewlett Packard Model 1720A oscilloscope with two HP 10016A probes or a Tektronix model 485 oscilloscope with two Tek P6053B probes.
- Digital Voltmeter with 6-digit integrating DVM with 1 volt resolution and 0.01% accuracy.
- Volt-Ohm-Meter Simpson 260 VOM or equivalent

Fairchild offers parts to its customers as another means of achieving maximum product utilization. Customers may purchase on a piece part or spares kit basis or use the repair or exchange programs.

The Sentry basic spare parts kits contains those components and circuit board types which are located in several positions throughout the system. For example, there are two "tester" pins of electronics on one pin electronics (P.E.) card and four tester pins of electronics on one Pin Control II board; thus, a 90-pin system with one test head would have 45 P.E. cards and 24 Pin Control II cards.

The supplemental spare parts kit contains those printed circuit board types which are the most complex and probably the most difficult to troubleshoot should the need arise. They are offered to minimize repair time for personnel who are not intimately knowledgeable of the machine at the device level. Test system user maintenance personnel also have telephone assistance available from the FTSG local Field Service office when necessary to aid in rapidly localizing a problem to the board level.

Under the FTSG repair program, customer-owned units are repaired for a percentage of the current board sale price. Restrictions are placed upon the age of the boards and their reparability in order to be eligible for the program.

An exchange program relieves customers of critical situations as soon as possible on current production boards. The customer can obtain a board on an "as available" delivery basis prior to Fairchild receiving the bad board. The customer pays full price for the new board and then is credited a percentage of the bad board's current purchase price.

**RECOMMENDED SPARE PARTS KIT
SENTRY BASIC**

Quantity	Part Number	Description
1	97340208	8K x 25 RAM Board
1	97166001	2 Bit Slic PCB Rev. 6 or Above
1	97435102	Pin Control 1 PCB
1	97234303	Pin Control 2 PCB
1	97234315	Local Memory PCB 2K x 16
1	97230313	Timing Gen. PCB
10	05036850	Relay, 22541A
2	05036860	Relay, 45041C
2	05037100	Relay, 55141A
3	05906001	PMU Relay 91211C05
3	05907001	Relay, 766070101670
10	05903103	Relay, 131741A 10 MHz P.E.
5	12014570	Lamp, 5V (EIR)
1	81006400	Fan, Pamotor
1	81006060	Fan, Muffin
1	97431201	Analog Interface
1	97435001	Universal Output Dr.

**SENTRY-PATTERN PROCESSOR
SPARE PARTS KIT**

Quantity	Part Number	Description
1	97234301	Data Out PCB
1	97234401	Datalog Buffer PCB
1	97234402	Load Control A PCB
1	97234403	Clock A PCB
1	97360101	Control Address PCB
1	97360104	Control Data PCB
1	97360107	Reg. Compare PCB
1	97360111	Address MUX PCB
1	97360112	Data MUX PCB
1	97360113	Data RAM PCB
1	97360114	Pipeline PCB
1	97360127	Topological Scrambler PCB
1	97360109	Index Register

Recommended Spare Parts Kit
Sentry Supplemental

Quantity	Part Number	Description
1	97420112	CPI #3
1	97420108	CPI 1A PCB
1	97340806	XDL Counter PCB
1	97340805	Phase Loop Counter PCB
1	97206007	T-Counter PCB
1	97420313	PMU Analog 1B PCB
1	97420314	PMU Analog 2 PCB
1	97234306	Status and Mode PCB
1	97234304	Mem. Add. D PCB
1	97234305	Mem. Add. C PCB
1	97234314	Timing Ref. Distr. PCB
1	97340826	RVS PCB
1	97340825	DPS PCB
1	97206105	1 Amp Buffer PCB
2	97234309	Sequencer
1	97234302	Dual Test Rate
2	97234307	Clock
1	97034308	Clock 2M MAS/SC.
1	97234313	Time Base
1	97234319	Rank C Memory
1	97234312	Memory Address B
1	97234311	Memory Address A
1		Status & Mode

Sentry Acceptance Procedures

System conformance to the acceptance procedure described in this section for the Sentry performance and acceptance are verified. The system acceptance tests are run prior to system shipment and at the time of system installation. Acceptance procedure is comprised of the following items.

- A. Inventory/verify all items to be shipped (except those specifically approved to be shipped later).

- Record serial numbers of major modules
- Verify that documentation sets are available
- Verify software components are on disc by entering SET DIF'.PSLIP'

- B. Verify CPU and CPU memory by entering the following command from the VKT:

SET DIF'.CPU2'.

The diagnostics listed below will run automatically.

- INSF2 - CPU Instruction Check
- MEMF2 - Memory diagnostic
- XNDF2 - Index register diagnostic
- ATXF2 - Index register diagnostic
- PYRF2 - Pyramid adder check
- RELF2 - Relative memory address diagnostic
- MEMRD - Memory Random Data

- C. Verify peripheral operation by executing the following diagnostics:

- Disc - QDISC (3 runs)
- Mag. Tape - MGT DIA
- Card Reader - CRDIA
- Line Printer - appropriate line printer diagnostic
LPDIA - High-speed line printer
LSDIA - Low-speed line printer
- Video Keyboard Terminal - TTYDI
Video Keyboard Terminal #2 - TTYD2

- D. Verify system performance with the Sentry Tester Verification Program (TVFY), which self-tests the integrity of data paths, functions, and D.C./Dynamic accuracies of the Sentry. the Sentry

systems equipped with the high speed stations are verified with LTVFY. This program accounts for tolerances of both the self-stimulus and measurement accuracy specifications of the system. The tests included in TVFY are listed in Table 11-1.

- E. To further ensure system performance, exercise the system in its operating mode by executing standard FST device programs on each test head without any failures. The two programs to be executed incorporated both N and N^2 functional patterns.

If the system is configured without the Hardware Pattern Generator option, test it with the R93410 TTL 256 x 1 TTL RAM device test program.

The program includes Checkerboard, Column Bar, Row Bar, Diagonal, and Ping Pong patterns. "R93410" also has Solid, Parity, Shift, Chip Select Access Time, and Write Recovery Time patterns.

"R93410" runs DC tests for input clamp voltage, input low current, input high current, output low voltage, and output leakage.

If the system is configured with the hardware pattern generator option, verify pattern generator operation using PDIAG and the device test program: H93410 TTL 256 x 1 RAM.

"H93410" includes Solid, Checkerboard, Column Bar, Row Bar, Diagonal, Parity, Shift, Ping Pong, Chip Select Access Time, and Write Recovery Time patterns. It also does the DC parametric tests for input clamp voltage, input low current, input high current, output low voltage, and output leakage.

- F. To verify pin driver skew specifications execute the FACTOR program SKEW6. Use a high-frequency oscilloscope with one pin as reference and visually check the remaining tester pins for skew relative to the reference pins.

Place Probe #1 on Tester Pin/Output and sync the scope off this input. A performance board is not used in this procedure.

Sequentially place probe #2 on remaining pins and observe time difference between the two waveforms at both leading and trailing edges. Maximum spread is 2 ns from pin 1, the reference pin, adjust as required.

Table 11-1 TVFY Acceptance Test

Test	Description
1	Mainframe Short Register Test. All short registers are exercised with floating ones and zeroes with crosstalk tests.
2	Mainframe Time Delay Test. All time delay registers are tested for correct time delay.
3	Station Controller Long Register Test. All long registers are exercised with floating ones and zeroes with crosstalk tests.
4	Local Memory Test. The local memory is exercised with checkerboard, checkerboard complement, all ones, all zeroes, and address test.
5	Memory Control Test. The memory control hardware is tested by executing minor and major loop.
6	Local Memory Cycle Steal. The local memory is tested for the ability to alter locations while in a continuous loop test.
7	Loop Counter Test. The major and minor loop counters are tested to ensure proper operation.
8	Test Head Leakage Test. All tester pins are tested for leakage and comparator bias current.
9	PMU Test. The precision measurement unit is tested for D.C. and dynamic accuracy in all force and sense ranges.
10	PMU Clamp and relay driver test. The PMU clamp is verified at various voltage levels. All odd utility drivers from pin 31 to pin 59 are tested.
11	I/O switch and I/O mode Test. Each Data Driver is tested for correct I/O switch operation in DA/DB modes and in IOMODE/IOMD3.
12	Internal Node Test. All RVS's and DPS's are tested for D.C. accuracy at the internal mode.
13	Test Head D.C. Test. The D.C. accuracy of the functional drivers is tested.
14	Driver Impedance Test. The output impedance of all drivers is tested at full-rated current.
15	Pin Electronics Function Test. The drivers and comparators are tested functionally to verify dynamic accuracy and functional fail logic.
16	Pin Control II Test. Ignore fail, chain 2, chain 4, ignore fail by count, XOR, MUX, IMASK, RTO mode are verified.
17	Timing Generator Assignment Test. All possible combinations of timing generator and pin assignments are tested to verify the decoder logic and utility relay performance.
18	Timing Generator Delay and Width Test. Each timing generator delay and width counter is tested in all ranges.
19	Match Mode Test. The match mode function is tested in a functional program to ensure that a match condition is detected correctly.
20	Latch Mode Test. The latch mode function is tested to ensure that the comparator register will accumulate fail data while the latch is enabled.
21	Comparator Relay Test.
30	Burn-In Test Repeated at Requested Rep Rate. All tests, 1 through 20, are exercised during each cycle of burn-in. Summary printout indicates results.

-
- G. To test the Pattern Processor (PPM), run the Pattern Processor Diagnostic (PPOD) with a repetition rate of one second for a minimum of three times. The tests included are listed in Table 11-2.

Execute the pattern processor device program P93410 with performance board with Option 5 selected (repeated execution) for a minimum of 3 times. Patterns included in the P93410 are:

- Spiral Complement March
- Diagonal March
- Checkerboard Complement March
- Ping-Pong
- Checkerboard Complement March with Refresh
- Checkerboard Complement March with Data Extension.

Remove the 93410 device and insert the '4027' test program

Execute the test a minimum of 3 times noting that the device passes each test.

The P4027 test program utilizes the PPM to generate the following test patterns:

- Solid zeros and ones
- Sliding diagonal
- Walking column bar
- Walking row bar
- Butterfly
- Checkerboard complement march with active and passive refresh row disturb
- Ping Pong with the true and complement data

Table 11-2 Pattern Processor Diagnostics (PPOD)

Test	Description
1	Read/write the registers associated with PPM.
2	Test the PPM Control RAM.
3	Test the address generator which provides the X/Y coordinate addressing.
4	Test the data generator X and Y parity generators and address comparators.
5	Test the address and data signals at the test heads.
6	Test the alternate TG4.
7	Test the topological RAM memory.
8	Test the data RAM memory.
9	Test the Data RAM address, shifter, and pseudo shifter modes.

-
- H. To test the Sequence Processor (SPM), execute the Sequence Processor Diagnostic (SPDG) in Mode R (all tests with internal sync, then all tests with external sync) for a minimum of three times. The TVFY load board must be mounted for this test. (Mode RL can also be used to give summary on the line printer.) The tests included in SPDG are listed in Table 11-3.

Execute sequence processor device program S2533. Select Test Number 4 and run 10 times. Use a known good device and performance board 97231028. The following tests are included within program S2533:

- Clock Burst Normal.
- Clock burst match by count, DC time, and sequential match of 12.
- Clock burst mix.
- 16 levels of normal subroutines.
- Match mode subroutine by command DC time.

On those systems equipped with the high speed test station:

Execute the device program 'S2533' using a known good device and the performance board verify the SPM.

Table 11-3 Sequence Processor Diagnostic (SPDG)

Test	Description
1	Terminate Test. Tests for correct local memory termination.
2	Test each of the local memory commands: LGOTO, LCALL, LEND, LSET, LSETI, LSETIX.
3	Clock Burst Test.
4	Loop Counter, Stack, and Stack Pointer Test.
5	MultiLevel Loop Test.
6	Continuous Mode Test.
7	Local Memory Modification Test.
8	Match Mode Test.
9	Sequence of Commands Test.

Terms and Conditions of Sale

These terms and conditions apply to all quotations made and purchase orders accepted for systems and products offered for sale by Fairchild Test Systems Group, a Division of Fairchild Camera and Instrument Corporation, hereinafter referred to as Seller, and represent the sole understanding between the Seller and customer, hereinafter referred to as Buyer.

12.1 Order Acceptance

Buyer's purchase order is accepted only when Seller issues an order acknowledgement confirming to Buyer product, quantity, price and payment terms, as well as delivery dates, shipping destination and special packing instructions. Acceptance of Buyer's order is on the condition that these terms and conditions or any changes in these terms and conditions of sale do not apply unless agreed to in writing by Seller. Prices acknowledged are firm and are not subject to audit.

12.2 System Acceptance

Acceptance will occur upon completion by Seller of the Standard system acceptance procedures, Section 11 above, at the Seller's designated facility.

Buyer will be given an opportunity to witness the performance of the acceptance procedures. If Buyer fails to attend or designate a representative, Seller will appoint a member of its Quality Assurance staff to act as agent for Buyer and to issue a Quality Assurance Certificate of Acceptance.

12.3 Delivery

All sales are made F.O.B. point of shipment at Seller's facility. Seller's title and risk of loss pass to Buyer upon tender of delivery of system or product to carrier at shipping point in good condition, the carrier acting as Buyer's agent.

If Buyer does not provide instructions specifying the method of shipment to be used, the Seller will exercise its own discretion and procure insurance for the benefit of Buyer at Buyer's expense.

12.4 Shipment

Seller will manufacture in accordance with the planned shipping date, as confirmed in Seller acknowledgement. Final shipping date will be established based upon date of system acceptance.

It is understood that factors beyond Seller's control may cause delays in shipment. Seller in such cases will notify Buyer promptly and use its reasonable efforts to reschedule shipments. In no event will Seller be liable for special or consequential damages.

Seller reserves the right to make partial shipments with the consent of Buyer, which will not be unreasonably withheld, and invoices will be issued accordingly by purchase order line item.

12.5 System Installation and Demonstrations

Seller will install and demonstrate the system at the Buyer's facility designated as the destination to ensure proper operation and performance in accordance with Seller's standard installation and demonstration procedure.

12.6 Terms of Payment

12.6.1 Domestic USA and International Plan A

Seller will invoice Buyer on the delivery date, which is the day the system or product is tendered to the carrier at the shipping point. All invoices will be for the confirmed purchase price and due and payable within 30 days of invoice.

In the event that installation and demonstration of the system in accordance with Seller's standard installation and demonstration procedure is not accomplished within 30 days after delivery for a reason attributable to Seller, Buyer may request and Seller will grant a credit of 20% against the purchase price. Buyer may withhold said 20% which will be due and payable by the Buyer within 30 days of system installation and demonstration.

If there is a material change in the credit rating of the Buyer which causes delivery on the terms of payment acknowledged to be unjustified, the Seller may require full or partial payment in advance. In the event of bankruptcy or insolvency laws, the Seller shall be entitled to cancel any order then outstanding and shall receive reimbursement for cost and profit for items so cancelled.

12.6.2 International Plan B

All quotations are made and orders are accepted on the basis of establishment of an irrevocable letter of credit issued by a bank, acceptable to Seller, payable in United States Dollars available by sight draft upon presentation of copies of the Commercial invoice, required U.S. Export License(s) Packing List, and Bill(s) of Lading indicating delivery to the appropriate carrier/forwarder.

12.7 Taxes

All sales, use, excise or similar taxes applicable to the manufacture or sale of the systems or products shall be added to the purchase price and shall be paid by the Buyer. In lieu thereof, where applicable, the Buyer shall provide a tax exemption certificate accept to the taxing authorities.

12.8 Patents

If any suit or proceedings are brought against Buyer claiming that any system or product or any part thereof manufactured by Seller and furnished under the purchase order constitutes an infringement of any patent of the United States, Seller shall defend at its expense, provided Buyer promptly notifies Seller in writing of any such suit or proceedings and gives authority, information and assistance (at Seller's expense) for the defense or settlement of same. Seller shall pay all damages and costs awarded therein against the Buyer. In case said product, or any part

thereof, is in such suit held to constitute infringement and the use of said product or part is enjoined, the Seller shall at its own expense, either procure for the Buyer the right to continue using said product or part, or replace same with non-infringing product or modification, or remove said and refund the purchase price and the transportation and installation costs thereof. The foregoing states the entire liability of the Seller for patent infringement by the said system or product(s) or any part thereof.

The Buyer shall hold the Seller harmless against any expense or loss resulting from infringement of patents or trademarks arising from compliance with Buyer's designs, specifications, or instructions. The sale of products by the Seller does not convey any license, by implication, estoppel, or otherwise under patent claims covering combinations of said products with other devices or elements.

12.9 Assignment

Buyer or Seller shall not assign the order or any interest herein or any rights thereunder without the prior written consent of the other party.

12.10 Warranty

Seller warrants equipment of its manufacture against defective material or workmanship for a period of one year. The warranty period for systems starts when installation and demonstration is completed and on the shipping date for all other products. Systems are repaired free of charge at the installation site for the first 90 days. For the remainder of the warranty period, all defective products, subassemblies or components will be repaired or replaced free of charge for service or materials if returned freight prepaid to the Seller's factory or service depot. Seller will bear freight charges for shipment after repair or replacement.

This warranty applies only to normal use and does not extend to expendable items such as lamps, fuses, etc., or mechanical parts failing from normal usage. In the case of equipment not manufactured by Seller, Seller will replace or repair equipment free of charge during the first 90 days following system installation and demonstration.

THIS WARRANTY IS EXPRESSED IN LIEU OF ALL OTHER WARRANTIES OR REPRESENTATIONS EXPRESSED, IMPLIED, OR STATUTORY, INCLUDING THE IMPLIED WARRANTIES OF FITNESS FOR A PARTICULAR PURPOSE, OR MERCHANTABILITY. THIS WARRANTY MAY BE ASSERTED BY BUYER ONLY AND NOT BY BUYER'S CUSTOMERS. IN NO EVENT SHALL SELLER BE LIABLE FOR CONSEQUENTIAL OR SPECIAL DAMAGES.

12.11 System Support

Service support and replacement parts for both the standard system manufactured by Seller, and other equipment supplied with the system, or equivalent, will be available in accordance with Seller's published rates for service and materials for a period of five (5) years from date of system acceptance subject to Warranty above).

For an additional five (5) years the Seller will make reasonable efforts to continue to provide the foregoing system support.

Sentry VIII Specifications

Reference Voltage Supply
Device Power Supplies
Timing Generator
Precision Measurement Unit
2V/2mV RVS, DPS, PMU Options
Pin Electronics High Voltage Data Driver and Clock Mode
Pin Electronics High Voltage Output Mode (Comparator)
Pin Electronics High Voltage Input/Output Mode
Pin Electronics High Voltage Power Supply Mode
Pin Electronics HighSpeed Output Mode (Comparator)
Pin Electronics High Speed Data Driver and Clock Mode

Reference Voltage Supply (RVS)

Description The RVSs provide the 1 and 0 logic levels to the drivers and detectors.

Specifications

REFERENCE VOLTAGE SUPPLY (RVS)

The RVS is a programmable Reference Voltage Supply with 10 bits force magnitude, 2 bits for range, 1 bit for polarity.

Range	Forcing Range	Resolution	Accuracy (1% of programmed value)
2	0 to ± 10.23 V	10 mV	0.1% ± 10 mV
3	0 to ± 30.72 V (5 MHz) 0 to ± 16.00 V (10 MHz)	40 mV	0.1% ± 40 mV

SYSTEM REPEATABILITY/NOISE: ± 10 mV max. (Allowed in Internal Node Check)

Device Power Supplies (DPS)

Description

The DPSs provide both programmable voltages and currents to the test station for parametric testing. The DPSs also include a current trip detector (DPT) which allows programming in two ranges and acknowledges current flow direction according to polarity of the DPS.

NOTE

The following specifications apply when the DPSs are brought to the test head through the performance board rather than the pin electronics

Specifications

Voltage Force or
Voltage Trip

Range	Max Load	Least Significant Digit	Accuracy % of Value
LOW			
± 0 to ± 10.23 V*	± 1 A	10 mV	0.1% ± 1
HIGH			
± 0 to ± 40.92 V*	± 1 A	40 mV	0.1% ± 1 bit

Regulation

No load to full load ± 20 mV**

Time Response

Settling to 1% in 1 ms

Overshoot 1% of step value change into resistive load

Current Trip Out

See DPT (Digitally Programmed current trip detector)

*Relative to chassis ground

**When force/sense is tied at the load board.

Current Trip or Force

Range	Max Load	Least Significant Digit	Accuracy % of Value
Bit 11 = 1	0-1 A (magnitude)	1 mA	$\pm 1.5\% \pm 2$ bits
Bit 11 = 0	0-0.1 A (magnitude)	0.1 mA	$\pm 1.5\% \pm 2$ bits

Bit 12 = 1 indicates trip if current > programmed value.

Bit 12 = 0 indicates trip if current < programmed value.

Response Time

Tracks supply load with no greater than 1 microsecond delay. Trip is automatically inhibited for 3 ms during forcing changes.

Trip level activates system interrupt.

Precision Measurement Unit (PMU)

Description

The PMU under program control can be connected to an individual DUT for quantitative voltage or current measurement. The PMU voltage clamp allows protection from overvoltage due to programming errors, or voltage compliance problems.

Specifications

VOLTAGE CLAMP TABLE

Volts Low Range (PSL=0)	Volts High Range (PSL5=0)
± 1.5	± 3
± 4.5	± 4
± 7.5	-15
±10.5	-21
-13.5	-27
-16.5	-33
-19.5	-39
-22.5	-45
-25.5	-51
-28.5	-57
-31.5	-63
-34.5	-69
-37.5	-75
-40.5	-81
-43.5	-87
-46.5	-93

NOTES

1. PSL4 = 0, no clamp
2. Voltage clamp values are with respect to TCOM.
3. The clamp values are slightly lower, if a small current is forced (less than 10 least significant counts of any current ranges).

Specifications

SENTRY STANDARD PRECISION MEASUREMENT UNIT (PMU) SPECIFICATIONS FORCE VOLTAGE/MEASURE CURRENT

Range	Forcing Range	Resolution	Rise Time* (10-90%) (All Measuring Ranges)	Accuracy (% of Programmed Value)	Overshoot* (% of Programmed Value) (All Measuring Ranges)
1	0 to ± 1.023 V	1 mV	100 μ s	$\pm .3\% \pm 4$ mV	<15%
2	0 to ± 10.23 V	10 mV	200 μ s	$\pm .15\% \pm 10$ mV	<5%
3	0 to ± 40.92 V	40 mV	400 μ s	$\pm .15\% \pm 40$ mV	<1%
4	0 to ± 102.30 V	100 mV	600 μ s	$\pm .15\% \pm 100$ mV	<1%

Regulation: No load to full load of the current range $\leq \pm 40$ mV/100 mA.

Leakage: The PMU measurement system leakage resistance shall not be less than 2000 M Ω to system ground at less than 50% relative humidity and 25°C ambient temperature at the station inlet (leakage current increases 0.5 nA/V). (Leakage error is additive to listed specifications.)

Tester Common: TCOM: -11V ± 3 mV on 5 or 10 MHz test station. 0 V on the high speed test station.

Repeatability: For 100 consecutive measurements, ± 4 counts when forcing or measuring in the 1 V or 1 μ A ranges, ± 1 count in all remaining ranges.

Required Measurement Delay** (in msec) Forcing Ranges 1/2/3/4							
Range	Measuring Range	Least Significant Bit	Voltage Compliance	Accuracy*** (% of Measured Value)	Typical Value	5 MHz Max Value	10 MHz Max Value
0	0 to ± 1.023 μ A	1 nA	-93.0 V	$\pm .5\% \pm 10$ nA	4/5/20/40	10/15/50/100	10/15/50/120
1	0 to ± 0.1023 mA	0.1 μ A	-93.0 V	$\pm .15\% \pm 200$ nA	0/0/0.5/1	0/0/1/2	1/1/1.5/3
2	0 to ± 10.23 mA	10 μ A	-93.0 V	$\pm .15\% \pm 20$ μ A	0/0/0.5/1.5	0/0/1.5/3	0/0/1.5/3
3	0 to ± 102.3 mA	100 μ A	-93.0 V	$\pm .2\% \pm 200$ μ A	0/0/0.5/1.5	0/0/1.5/3	0/0/1.5/3

FORCE CURRENT/MEASURE VOLTAGE

Range	Forcing Range	Least Significant Bit	Rise Time* (10-90%) (All Measuring Ranges)				Voltage Compliance	Accuracy*** (% of Programmed Value)	Overshoot* (% of Measuring Ranges) 1/2/3/4/
			1 (1V)	2 (10V)	3 (40V)	4 (100V)			
0	0 to ± 1.023 μ A	1 nA	700 μ s	5 ms	20 ms	45 ms	-93.0 V	$\pm .5\% \pm 10$ nA	20/5/3/3
1	0 to ± 0.1023 mA	0.1 μ A	110 μ s	250 μ s	500 μ s	800 μ s	-93.0 V	$\pm .15\% \pm 200$ nA	20/5/3/3
2	0 to ± 10.23 mA	10 μ A	110 μ s	250 μ s	500 μ s	800 μ s	-93.0 V	$\pm .15\% \pm 20$ μ A	20/5/3/3
3	0 to ± 102.3 mA	100 μ A	110 μ s	250 μ s	500 μ s	800 μ s	-93.0 V	$\pm .15\% \pm 200$ μ A	20/5/3/3

Required Measurement Delay**—ms Forcing Ranges 0/1/2/3						
Range	Measuring Range	Least Significant Bit	Accuracy (% of Measured Value)	Typical Value	5 MHz Max Value	10 MHz Max Value
1	0 to ± 1.023 V	2 mV	$\pm .3\% \pm 4$ mV	3/0/0/0	8/0.5/0.5/0.5	8/0.5/0.5/0.5
2	0 to ± 10.23 V	10 mV	$\pm .15\% \pm 20$ mV	20/0/0/0	35/1/1/1	48/1/1/1
3	0 to ± 40.92 V	40 mV	$\pm .15\% \pm 40$ mV	80/2/1/0	130/6/2/2	190/6/2/2
4	0 to ± 102.30 V	100 mV	$\pm .15\% \pm 100$ mV	190/5/2/2	270/13/5/5	480/13/5/5

The measuring circuit will provide automatic down ranging to the range of best resolution when AUTO range is specified.

Programmable Clamp: Positive Clamp: -0.7 V to +9 V; Negative Clamp: +0.7 V to -V_c; Symmetrical Clamp: $\pm V_c$
VC Programmable (see Voltage Clamp Table: $\pm 10\% \pm 1$ V accuracy).

Capacitive Loading: .01 μ F maximum.

*With R_L = Voltage range/current range and slewing from 0 to 50% of the range.

**When forcing current Range 0/Range 1/Range 2/Range 3 or forcing voltage in Range 1/Range 2/Range 3/Range 4, respectively and slewing from 0 to 50% of the range and a resistive load equal to the voltage range/current range. This delay gives accuracies within 0.6% of full scale compared to the value measured in manual mode (static). The programmed delay is in parallel to a fixed hardware delay of about .5 msec.

***For longer delay (1), $\pm 0.5\% \pm 5$ nA accuracy can be achieved on 1 μ A range.

2 V/2 mV RVS, DPS, PMU option

Description

The 2V/2 mV option provides increased voltage resolutions for the 5 and 10 MHz test stations. It incorporates 2 V/2 mV range into the RVS and DPS and changes 1 V/1 mV range of PMU to 2 V/2 mV.

Specifications

REFERENCE VOLTAGE SUPPLY (RVS)

The RVS is a programmable Reference Voltage Supply with 10 bits force magnitude, 2 bits for range, 1 bit for polarity.

Range	Forcing Range	Resolution	Accuracy (1% of programmed value)
1	0 to ± 2.046 V	2 mV	0.1% ± 2 mV
2	0 to ± 10.23 V	10 mV	0.1% ± 10 mV
3	0 to ± 16.00 V (10 MHz) 0 to ± 30.72 V (5 MHz)	40 mV	0.1% ± 40 mV

SYSTEM REPEATABILITY/NOISE: ± 10 mV max. (Allowed in Internal Node Check)

DIGITALLY PROGRAMMED POWER SUPPLY (D.P.S.), 2 V/2 mV OPTION

The DPS is a Programmed Power Supply with 10 bits for magnitude, 2 bits for ranges, 1 bit for polarity, 2 V/2 mV option (Range 1) is added to Voltage Forcing Mode only.

VOLTAGE FORCING

Range	Forcing Range	Resolution	Accuracy (% of programmed value)
1*	0 to ± 2.046 V	2 mV	0.1% ± 2 mV
2	0 to ± 10.23 V	10 mV	0.1% ± 10 mV
3	0 to ± 40.92 V	40 mV	0.1% ± 40 mV

SYSTEM REPEATABILITY/NOISE: ± 10 mV max. (Allowed in Internal Node Check)

*No voltage trip/current trip in RANGE 1

Specifications

SENTRY OPTIONAL 2 V/2 mV PMU SPECIFICATIONS FORCE VOLTAGE/MEASURE CURRENT

Range	Forcing Range	Resolution	Rise Time* (10-90%) (All Measuring Ranges)	Accuracy (% of Programmed Value)	Overshoot* (% of Programmed Value) (All Measuring Ranges)
1	0 to ± 2.046 V	2 mV	100 μ s	$\pm 3\%$ ± 8 mV	<15%
2	0 to ± 10.23 V	10 mV	200 μ s	$\pm 15\%$ ± 10 mV	<5%
3	0 to ± 40.92 V	40 mV	400 μ s	$\pm 15\%$ ± 40 mV	<1%
4	0 to -102.30 V	100 mV	600 μ s	$\pm 15\%$ ± 100 mV	<1%

Regulation: No load to full load of the current range ≤ 40 mV/100 mA.

Leakage: The PMU measurement system leakage resistance shall not be less than 2000 M Ω to system ground at less than 50% relative humidity and 25°C ambient temperature at the station inlet (leakage current increases 0.5 nA/V). (Leakage error is additive to listed specifications.)

Tester Common: TCOM: -11 V ± 3 mV

Repeatability: For 100 consecutive measurements, ± 4 counts when forcing or measuring in the 1 V or 1 μ A ranges, ± 1 count in all remaining ranges.

Required Measurement Delay** (in msec) Forcing Ranges 1/2/3/4

Range	Measuring Range	Least Significant Bit	Voltage Compliance	Accuracy*** (% of Measured Value)	Typical Value	5 MHz Max Value	10 MHz Max Value
0	0 to ± 1.023 μ A	1 nA	-93.0 V	$\pm .5\%$ ± 10 nA	4/5/20/40	10/15/50/100	10/15/50/120
1	0 to ± 0.1023 mA	0.1 μ A	-93.0 V	$\pm .15\%$ ± 200 nA	0/0/0.5/1	0/0/1/2	1/1/1.5/3
2	0 to ± 10.23 mA	10 μ A	-93.0 V	$\pm .15\%$ ± 20 μ A	0/0/0.5/1.5	0/0/1.5/3	0/0/1.5/3
3	0 to ± 102.3 mA	100 μ A	-93.0 V	$\pm .2\%$ ± 200 μ A	0/0/0.5/1.5	0/0/1.5/3	0/0/1.5/3

FORCE CURRENT/MEASURE VOLTAGE

Range	Forcing Range	Least Significant Bit	Rise Time* (10-90%) (All Measuring Ranges)				Voltage Compliance	Accuracy*** (% of Programmed Value)	Overshoot* (% of Measuring Ranges) 1/2/3/4/
			1 (1V)	2(10V)	3(40V)	4(100V)			
0	0 to ± 1.023 μ A	1 nA	700 μ s	5 ms	20 ms	45 ms	-93.0 V	$\pm .5\%$ ± 10 nA	20/5/3/3
1	0 to ± 0.1023 mA	0.1 μ A	110 μ s	250 μ s	500 μ s	800 μ s	-93.0 V	$\pm .15\%$ ± 200 nA	20/5/3/3
2	0 to ± 10.23 mA	10 μ A	110 μ s	250 μ s	500 μ s	800 μ s	-93.0 V	$\pm .15\%$ ± 20 μ A	20/5/3/3
3	0 to ± 102.3 mA	100 μ A	110 μ s	250 μ s	500 μ s	800 μ s	-93.0 V	$\pm .15\%$ ± 200 μ A	20/5/3/3

Required Measurement Delay**—ms Forcing Ranges 0/1/2/3

Range	Measuring Range	Least Significant Bit	Accuracy (% of Measured Value)	Typical Value	5 MHz Max Value	10 MHz Max Value
1	0 to ± 2.046 V	2 mV	$\pm .3\%$ ± 8 mV	3/0/0/0	8/0.5/0.5/0.5	8/0.5/0.5/0.5
2	0 to ± 10.23 V	10 mV	$\pm .15\%$ ± 20 mV	20/0/0/0	35/1/1/1	48/1/1/1
3	0 to ± 40.92 V	40 mV	$\pm .15\%$ ± 40 mV	80/2/1/0	130/6/2/2	190/6/2/2
4	0 to -102.30 V	100 mV	$\pm .15\%$ ± 100 mV	190/5/2/2	270/13/5/5	480/13/5/5

The measuring circuit will provide automatic down ranging to the range of best resolution when AUTO range is specified.

Programmable Clamp: Positive Clamp: -0.7 V to $+9$ V; Negative Clamp: $+0.7$ V to $-V_c$; Symmetrical Clamp: $\pm V_c$
VC Programmable (see Voltage Clamp Table: $\pm 10\%$ ± 1 V accuracy).

Capacitive Loading: .01 μ F maximum.

*With R_L = Voltage range/current range and slewing from 0 to 50% of the range.

**When forcing current Range 0/Range 1/Range 2/Range 3 or forcing voltage in Range 1/Range 2/Range 3/Range 4, respectively and slewing from 0 to 50% of the range and a resistive load equal to the voltage range/current range. This delay gives accuracies within 0.6% of full scale compared to the value measured in manual mode (static). The programmed delay is in parallel to a fixed hardware delay of about .5 msec.

***For longer delay (1), $\pm 0.5\%$ ± 5 nA accuracy can be achieved on 1 μ A range.

Timing Generator (TG)

Description Timing generators provide synchronization and timing for single or multiphase clock devices. They also provide fail strobe and data timing for functional testing.

Specifications

	Range	Full Scale	Programming Resolution
Test Rate Period Pulse	0	40 μ s	10 ns
	1	400 μ s	100 ns
	2	4 ms	1 μ s
	3	40 ms	10 μ s
Pulse Width or Delay	0	10 μ s	0.16 ns
	1	100 μ s	100 ns
	2	1 ms	1 μ s
	3	10 ms	10 μ s

Conditions for above:
Pulse width $\leq$ period
Pulse delay $\leq$ period
Pulse delay + width $\leq$ 2 periods

Accuracy of
Programmed Value Maximum: 0.5 ns

NOTE
The above times exclude the use of I/O switching

Pin Electronics High Voltage Data Driver and Clock Mode

Description

The data driver and clock provide the input voltage stimulus for the DUT.

Specifications

Drivers	As measured into a standard of 1 M in parallel with 50 pF* for data or 100 pF (for clock drivers, located three inches from the pin electronics output unless otherwise specified).
Output	10 MHz +6 V to -16 V (22 V p to p)
Accuracy	10 MHz $\pm 0.8\%$ ± 15 mV (10 V range) DC at 23°C $\pm 1\%$ C $\pm 0.08\%$ ± 25 mV (40 V range) DC at 23°C $\pm 1\%$ C for 7 hours ± 75 mV (≤ 3.75 V signal) $\pm 2\%$ (> 3.75 V signal) Relative to steady-state value at 50 ns from start time of voltage slew into an impedance of > 1 M Ω shunted by 10 pF*. Steady-state value is achieved ≥ 1 msec after starting time of voltage slew.
Resolution	10 MHz +6 V to -16 V
Stability	10 MHz For a change in ambient temperature of $\pm 7^\circ$ C from 23°C for a period of 30 days, the maximum drift is $\pm 0.1\%$ ± 15 mV in addition to the accuracy specification
Reference Voltage Input	Data Drivers One of two pairs of reference supplies: E1, E0, EB1, EB0. Clock Drivers One of two pairs of reference supplies: EA0, EA1, EC0, EC1
Voltage Slew Rate	10 MHz > 1.5 V/ns at 20 V p-p into 10 pF* in parallel with 1 M Ω . > 1 V/ns at 20 V p-p into 100 pF.* Measured at the 50% level.
Rise/Fall Time (10-90%)	10 MHz < 10 ns at 5 V p-p, < 20 ns at 20 V p-p (10 pF* load).
Overshoot/Undershoot	10 MHz ≤ 100 mV at 5 V p-to-p, ≤ 300 mV at 20 V p-to-p (10 pF load).
Minimum Pulse Width	10 MHz 20 ns at 5 V p-to-p (measured at the 50% points).

Specifications

Skew	10 MHz Adjustable to $<\pm 2$ ns on both edges at 5 V pk-to-pk using common reference supplies. Measured with no load and at the 50% level.
Source Resistance	10MHz $47\ \Omega \pm 6\ \Omega$ for ≤ 100 mA d.c. in data mode. $30\ \Omega \pm 5\ \Omega$ for < 100 mA d.c. in clock mode.
Load Current	± 100 mA d.c. (data or clock mode), ± 200 mA peak for < 100 ns.
Dissipation Limitation of Driver	800 mW maximum
I/O Switching	Switching from an input to an output or vice versa shall occur within 50 ns at the beginning of the cycle (for data pins only).

Pin Electronics

High Voltage Output Mode (Comparator)

Description	The comparator compares the output of the DUT to a programmed value (S0/S1/SA0/SA1).
Specifications	
Input Amplitude	10 MHz +6 V to -16 V (22 V p-to-p)
Accuracy of Threshold Voltage	10 MHz +0.08% $\pm$ 10 mV at 23°C $\pm$ 1°C ambient for 7 hours
Resolution of Threshold Voltage	10 MHz 10 mV in low range (+6 to -10.23 V) 40 mV in high range (+6 to -16 V)
Stability of Threshold Voltage	10 MHz (Maximum drift) $\pm$ 1% $\pm$ 15 mV These are in addition to accuracy specification, for a change in ambient temperature of $\pm$ 7°C from 23°C for a period of 30 days.
Comparator Hysteresis	10 MHz $\leq$ 10 mV pk-to-pk (PE board only)
Capacitive Loading	10 MHz <25 pF (typically 20 pF) as output only <45 pF (typically 40 pF) as I/O in the output state (exclusive of performance board) at 0 V in.
Input Bias Current	10 MHz $\leq$ 100 nA from +6 V to -12 V increasing monotonically to <2 μ A at -16 V.
Response Time	10 MHz Step inputs (t_r <1 ns) from 0.5 to 5 V. Propagation time through comparator will increase 3.5 ns when reference voltage is changed from 10% to 90% level of input signal.
Slew Rate	10 MHz >1.2 V/ns (negative going edge limitation only). Does not affect propagation time for input signals moving slower than 1.2 V/ns. Change in propagation time of one comparator with a change in input polarity or amplitude < $\pm$ 2 ns measured with the reference voltage set to the 50% level of the input pulse for amplitudes between 0.5 V and 20 V pk-to-pk, except when slewing rate limited.

Specifications

Skew (Among comparators for identical input):
10 MHz
<±2 ns, when reference level is between 10% and 90% of the input signal for amplitudes between 0.5 V and 20 V.

Threshold Voltage
Input

RVS pair S0/S1

Protection

Safe input voltage
10 MHz
+11 V to 23 V relative to TCOM
5 MHz
-34 V relative to TCOM

NOTE
Voltages outside this range are clamped by diodes at the driver and comparator provided the current is limited to <200 mA. No damage will occur if a pin is shorted to the chassis (+11 V), to a voltage programmed through any other PE board, or to the PMU. DPSs, however, when wired directly to the load board can provide ±1 ampere. This is potentially damaging to the PE so in no case should a DPS supply be directly connected to a PE pin. In an output mode, no harm shall occur if a pin using an RVS source is shorted to the chassis (system ground) or a voltage of -45 V relative to system ground.

Mask

Using additional local memory channel one of two mask registers resistors can be gated with the comparator with each functional test.

Local Memory	Mask Register
Channel Content	Used
0	MA
1	MB

Mark selection can change at the beginning of each test period.

Strobes

Minimum strobe width 10 ns
Allowable strobe region 10 MHz 10 ns after T0 to 10 ns before next T0 for input signals with zero rise and fall time
5 MHz:
10 ns after T0 to 35 ns before next T0

Pin Electronics High Voltage Power Supply Mode

Description

The driver is used as a power supply thus allowing the use of the DPS reference supplies as bias (100 mA steady-state). Tester Common (TCOM), DPS1, DPS2, and DPS3 are available reference supplies.

Specifications

Impedance	3 Ω maximum (typically 1 Ω)
Load current	100 mA
Format	Input pin
Voltage	5 MHz
	+6 V to -30 V relative to TCOM
	10 MHz
	+6 V to -16 V relative to TCOM
Amplitude	+51 V to -29 V relative to TCOM

NOTE

The DPS supply output is offset from TCOM by +11 V when used directly at the test head (not via the pin electronics) on the 5 MHz and 10 MHz test heads.

Pin Electronics High Voltage Input/Output Mode

Description

Allows complete independent changing of I/O definition of up to 15 pins with each test pattern.

Specifications

Mode Change

50 ns of T0 (test cycle start) or after a programmed delay depending on the timing generator programmed to the adjacent controlling pin.

Pin Electronics

High Speed Data Driver and Clock Mode

Description	The data driver and clock provide the input voltage stimulus for the DUT.	
Specifications		
Drivers	As measured into a load of 12.5 pF in parallel with 10 mΩ	
Output	Data driver	-1 V to +6 V
	Clock driver	-1 V to +16 V
Accuracy	VR1 level should be higher (more positive) than VR0. When VR1 is lower (more negative) than VR0 a 10 mV offset should be added to the accuracies: d.c. (no load) — 0.1% ±10 mV plus reference accuracy d.c. (with load) — refer to source resistance	
Stability	For a temperature of 23° ± 2° C for 30 days, maximum drift is ±0.1% ±15 mV in addition to accuracy specification.	
Reference Voltage Input	Data driver	Up to 2 pair (E0/E1, EB0/EB1) selected by S register
	Clock driver	Up to 2 pair (EA0/EA1, SA1/SA0) selected by S register
	NOTE SA0 and SA1 cannot be set above +6 V	
Rise/Fall Time	Data driver	Typically 2.0 ns for a 0.8 V pulse measured at 20% to 80% points.
	Volt pulse	Rise/Fall Time
	0.8	<2.5 ns at 10%-90% point
	2	<4 ns at 10%-90% point
	5	<5 ns at 10%-90% point
	NOTE The rise/fall time is measured with a sampling scope with a minimum bandwidth of 1 GHz and 10 pF load at the PE card contacts with comparator disconnected.	
	Clock driver	10 ns for a 12 V pulse with a 10 pF load at 10% to 90% points.

Specifications

Overshoot/Undershoot	Data driver 10% of programmed voltage with: 150 mV maximum for 0.8 V to 6 V pulse 90 mV maximum for 0.2 V to 0.8 V pulse NOTE These values reflect a measurement made with 10 m Ω with 12.5 pF probes. (Tektronix P6053B or equivalent) Clock driver 200 mV or 5% whichever is greater
Minimum Pulse Width (at 50%)	Data driver 8 to 10 ns 2-5 V 5 to 8 ns <2 V Clock driver 30 ns at 15 V pk-to-pk
Skew Among Drivers	Data driver Adjustable to $<\pm 1$ ns on both edges (+0.4 V to +2.4 V at 2 V pk-to-pk) using common RVS. Can be set to a resolution of better than 0.2 ns. Clock driver Adjustable to $<\pm 1$ ns on both edges at 12 V pk-to-pk using common RVS. Can be set to a resolution of better than 0.2 ns.
Source Resistance	Data driver 50 $\Omega \pm 5 \Omega$ with load current $\leq \pm 20$ mA (adjustable) Clock driver 30 $\Omega \pm 5 \Omega$ with load current $\leq \pm 20$ mA
Load Current	Data driver ± 20 mA d.c. over full voltage range (± 25 mA from 0V to +2.5 V) ± 80 mA a.c. Clock Driver ± 20 mA d.c. over full voltage range ± 80 mA a.c.
Protection	Protected up to ± 160 mA NOTE No damage will occur if a pin is shorted to the ground, to a voltage programmed through any other PE board, or to the PMU
Transient Settling Time	Data driver 50 mV or 2% whichever is greater relative to steady state value at 50 ns after starting time of voltage slew. Load is an impedance of 10 M Ω shunted by 12.5 pF. Steady state is ≥ 1 ms after starting time of voltage slew. Clock driver 200 mV or 2% relative to the steady state value at 50 ns after starting time of voltage slew. Load is an impedance of 10 M Ω shunted by 12.5 pF. Steady state is ≥ 1 ms after starting time of voltage slew.
Rise/Fall Linearity among Data Drivers	± 1 ns between pins with 0 skew measured at 2 V pk-to-pk pulse at the 10% to 90% points. ± 0.8 ns for 0.8 V pk-to-pk pulse measured at 20% to 80% points.
Voltage Slew Rate for Clock Drivers	>1 V/ns into 12.5 pF in parallel with 10 M Ω . (Typically 1.5 V/ns)
Minimum Voltage Swing on Clock Drivers	2 V Data Driver can be used for lower voltage swings

Pin Electronic

High Speed Data Drives and Clock Mode

Specifications

I/O Switching (Data
Driver Only)

Switching time

From input to output or output to input ± 10 ns at beginning of cycle
TO

Switching spike

> 0.8 V peak (typically 0.5 V) with load of $10\ \Omega$ in parallel with 12.5 pF
load

Switching time variation (I/O switch skew)

$\leq \pm 8$ ns between any pins

I/O output impedance $\approx 14\ M\Omega$

I/O controls

≤ 60 pins (Clock pins do not have an I/O switch)

Pin Electronics High Speed Output Mode (Comparator)

Description

The comparator compares the output of the DUT to a programmed value (S0/S1/SA0/SA1)

Specifications

Input voltage range	- 1 V to +6 V
Accuracy of threshold voltage	$\pm 0.1\% \pm 10$ mV (including reference accuracy)
Stability of threshold voltage	$23^{\circ}\text{C} \pm 2^{\circ}\text{C}$ for a period of 30 days maximum drift is $\pm 0.1\% \pm 15$ mV (in addition to accuracy specification)
Threshold voltage input	S0/S1, SA0/SA1 selected by S register
Protection	Protected up to ± 160 mA. NOTE No damage will occur if an input is shorted to the ground, to a voltage programmed through any other PE board, or to the PMU.
Comparator hysteresis	<10 mV pk-to-pk (pin electronics only)
Capacity loading	<20 pF as an output pin only <35 pF as an I/O pin in the output state NOTE Capacity loading is exclusive of performance board.
Input current	<100 nA for -1 V to +6 V
Comparator linearity	For input from 0.5 V pk-to-pk to 6 V pk-to-pk the change in propagation time (through comparator) is ≤ 1.2 ns when RVS is changed from 10% to 90% level of input signal. NOTE May vary when slewing rate limited
Slew rate	1.2 V/ns
Change in propagation time (with a change in input overdrive	<0.5 ns measured with RVS set to 50% level of input pulses from 0.5 V pk-to-pk to 6 V pk-to-pk NOTE May vary when slewing rate limited

Specifications

Skew among comparators (for identical input)	+1 ns (adjustable on both edges). Stability resolution is better than 0.2 ns.
Type of comparator strobe	Window
Allowable strobe region	10 ns after TO to 10 ns before the next TO
Mask	Using additional local memory channel one of two mask registers can be gated with the comparator with each functional test.

Local Memory	Mask Register
Channel Contents	Used
0	MA
1	MB

	Mask selection can change at the beginning of each test period.
Strobes	Minimum strobe width 10 ns
Reference select logic	Data driver E0/E1, EB0/EB1 Clock driver EA0/EA1 Comparator S0/S1, SA0/SA1
I/O switching (data pins only)	10 ns of TO

NOTE
Data driver may be switched from an input driver to an output comparator and vice versa in real-time.